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An Efficiednt Programmable Frequency Divider with Improved Division Ratio

N.Kirthika, Nisha Lali .R, Rejeesh.R S

Abstract: **The frequency divider is an important building block in today's high speed integrated circuits. Frequency divider is the most power hungry block in the communication system. Considering the scope of the frequency divider An Efficient Programmable Frequency Divider (PD) is presented. In this paper a shared counter with a small control circuit is exploited using Reduced Module Control Signal generator (RMCS).This will reduce the output load capacitance and the redundant counter operations in the divider. A Dual Modules Prescaler (DMP), which gives initial division ratio for the input signal by N or N+1.Dividing factor of the Efficient PD can increased by modifying DMP circuit for 16 or 17. A novel glitch less D flip-flop is also designed by considering the switching activities of the internal nodes of the flip-flop.**

Keywords-Dual modulus prescaler (DMP), programmable divider (PD), Reduced module control signal generator (RMCS).

I. INTRODUCTION

Frequency synthesizer is one of the major building blocks in modern communication synthesizers, which are widely used to implement various standards such as global systems for mobile communication, personal communications services, wideband code division multiple access, global positioning systems .In conventional phase-locked loop (PLL) based integer frequency synthesizer it generates a multiplied output frequency (F_{out}) from the reference frequency (F_{ref}), where the frequency F_{out} is controlled by the division ratio D. So a programmable frequency divider (PD) is an essential block in the high speed integrated circuit. The PD takes a dominant portion of the power consumption in the frequency synthesizer, reducing the PD power is becoming one of the fundamental design considerations .A dual modulus prescaler (DMP), which is the front-end of the PD, divides the high-frequency clock generated from the VCO. Since the DMP is operating at the highest frequency, it is the most power-hungry block in the PD. Moreover, the two redundant counters, namely programmable counter (PC) and swallow counter (SC) shown in Fig.1 increase the output load capacitance of the DMP, thus increasing the overall PD power consumption. In this paper the proposed programmable divider is designed and a Conventional Programmable Divider (PD) with two counters are used to compare with the efficient programmable divider. In the proposed PD the redundant operations of the two counters are effectively removed using single counter and a small control circuit. A glitch less DFF is also used to remove the glitches effectively from the DFF in the Dual modulus prescaler (DMP).

The rest of the paper is organized as follows: Section II describes the conventional programmable divider. Section III describes efficient programmable divider and section IV describes the design of DMP.

II. CONVENTIONAL PROGRAMMABLE DIVIDER

The conventional PD consists of DMP and Two counters a) Programmable counter (PC) b) Swallow counter (SC).The Dual Module Prescaler (DMP) divides the input signal (F_{in}) by either 'N' or 'N + 1' depending on the modulus control (MC) signal. Here DMP designed for N=4, which means that divide-by-5 (Div-5) and divide-by-4 (Div-4) operations are performed when the MC is low and high. The output from DMP is taken as D_{out}. The Swallow counter (SC) counts the rising edge of Dout up to the external input value S. When the SC counting value reaches S, modulus control (MC) is changed from low to high. Likewise, the PC counts the rising edge of D_{out} up to P and when the counter value reaches P, a reset pulse (RST) is generated from PC and both counters, SC and PC are reset. The divider can give a programmable division ratio 'D'.

$$D=S \times (N+1) + (P-S) \times N = N \times P + S \qquad (1)$$

Where N is given by DMP design P is fed to the PC and S is fed to the SC. Here P and S are designed for three bit value. P is generally greater than S. In the PD operation mode, since the DMP drives both the PC and SC, the output load capacitance of the DMP is large and the power dissipation becomes large as well. Moreover, both the PC and SC keep counting the rising edge of D_{out} until the counting number reaches P and S, respectively,

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***** Correspondence Author (s)
N.Kirthika*, Asst.Professor - M.E.VLSI DESIGN,Sri Ramakrishna Engineering College,Coimbatore, Tamilnadu, India,
(Email: kirthi.com@gmail.com).
Nisha Lali .R, PG Scholar Dept. of Electronics and Communication Engg, TKM Institute of Technology ,Kollam, Kerala, India,
(Email: nisha.lali.r@gmail.com).
Rejeesh.R S, PG Scholar - M.E.VLSI DESIGN,Sri Ramakrishna Engineering College, Coimbatore, Tamilnadu, India,
(Email: rs.rejeesh@gmail.com).

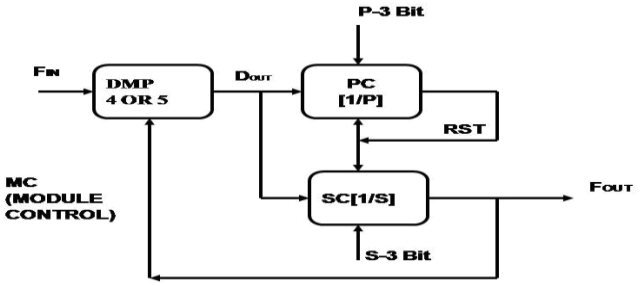

Fig.1 Conventional PD

where the simultaneous two counter operations leads to considerable power consumption.

A .Conventional PD simulation results

For obtaining a divisionfactor D=26, P value selected as 6 and S=2 (P>S). Here Dual Modulus Prescalar is designed for initial division ratio (N=4).Consider at the initial state the module control value (mc) is low and DMP divide the input signal by-5.So the output of DMP(Dout) contain single frequency pulse for five input pulse,Dout is feed to two counter Programmable counter(PC) and Swallow counter(SC) .For swallow counter(SC) when the Dout value become equal to the external 'S' value, the swallow counter(SC) change the MC value from zero to one.At the same time DMP will perform Div-by-4 operation.The PC already finished two count and it continues to count till the count value equal to 6.When the PC counts reaches 6 (P=6) a reset signal is generated from PC . Both PC and SC reset and the circuit give single frequency for 26 pulses that means a divider by factor(D) of 26.

B .Disadvantage

Since DMP has to drive two counters in parallel in the conventional architecture, these two counters operate simultaneously at its maximum operating frequency. This may result in redundant power consumption and area. Fanout required for the DMP is also high. Counter operation required more power consumption so here two counters are working parallel.

III. EFFICENT PROGRAMMABLE DIVIDER

Here a new architecture of a low power programmable divider for multi-standard frequency synthesizer, using reset and modulus control signal (RMS) generator. This divider involves only one counter, so that fanout of DMP is reduced and the duplicated counter operation is reduced as compared to conventional PD.

A .Architecture of efficient PD

The block diagram of proposed programmable divider consists of DMP, Up-counter (UC), Multiplexer (MUX), RMS generator in Fig 2.The DMP divides the input signal Fin by either N or N+1 depending on modulus control (MC) signal value, and generates Dout. In this project DMP is designed for N=4 and then modified for N=16 for getting higher dividing factor. It will perform divide-by-4 (Div-4) when MC is high and divide-by-5 (Div-17) when MC is low. The Up Counter (UC) which increase the counter output (Cout) on the rising edge of Dout and reset Cout asynchronously when reset (RST) is high. The 'MUX' select signal which value is equal to MC . When MC signal is low MUX output Mout should be 'S' which means UC counts the rising edge of Dout until S value. If both the count value(Cout) and S values become equal, RMS generator changes MC value from low to high. After the toggle DMP changes divide ratio from Div-5 to Div-4 and MUX select P value.

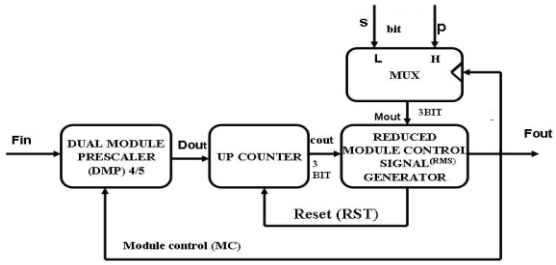

Fig.2 Block Diagram Of Efficient PD.

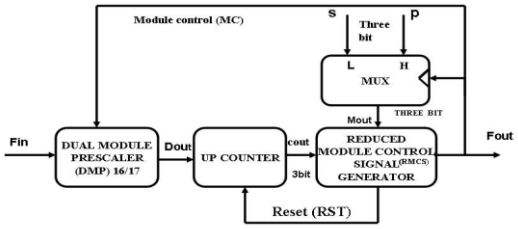

Fig.3 Block Diagram of Improved PD

Then, UC counts the rising edge of Dout until P value, if Dout and P values become equal, RMS generator changes MC value from high to low and generates high reset (RST) signal which resets Cout to zero. Thus, UC again counts rising edge of Dout from zero. As the processes described above repeated, the Efficient PD gives divide-by-D value.

$$D=S\times (N+1) + (P-S) \times N=N \times P + S \quad (2)$$

B. Design of Reduced Module Control Signal Generator (RMCS)

The RMCS generator consisting of an Equality detector, State machine in Fig.3.The equality detector generates a high equality signal (Eout) when the counting value (CNT) reaches the external control value, S and P. The state machine generates two control signals, MC and RST, for PD operations. Therefore the proposed PD adopts only a shared counter instead of the two counters used in the conventional programmable divider.

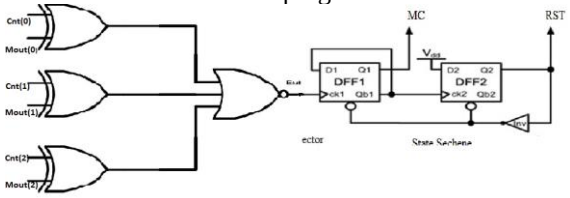

Fig.4 RMCS generator

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The operation of the RMCS generator when S = 2 and P = 6. DFF1 toggles at every rising edge of Eout and it changes the state of MC that mean Eout goes high every counter value became 2 and 6. At the first rising edge of Eout, the division ratio changes from Div-5 to Div-4, and at the second rising edge, the division ratio changes reversely from Div-4 to Div-5. DFF2 latches Vdd when the MC is changed from high (Div-4) to low (Div-5) and it generates a high RST signal to reset DFF1, DFF2.

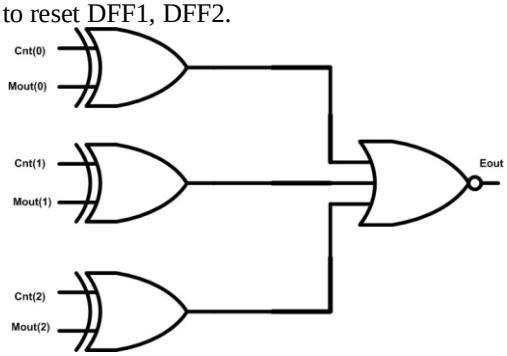

Fig.5 Equality detector for 3bit inputs

IV. DESIGN OF DUAL MODULUS PRESCALAR FOR N=4

The DMP block operates at the high speed in the frequency synthesizer and a large portion of the power is consumed in the PD. Fig. 4.4 shows the block diagram of the DMP, which consists of three DFFs and two logic gates. The MC signal is used to select the Div-4 or Div-5 function. In the Div-4 operation as shown in Fig. 5b, the input of the DFF3, which goes to D3, is always low. Thus, the DFF3 does not toggle.

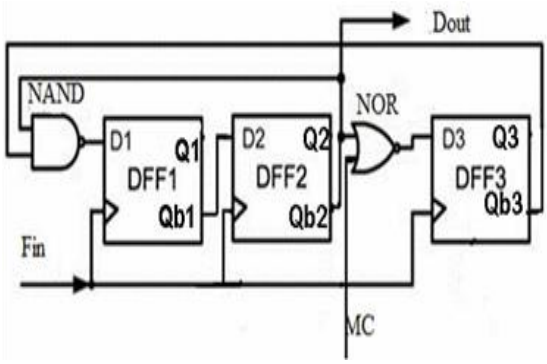

Fig.6 Block Diagram Of DMP

V. DESIGN OF DMP FOR N=16

The DMP block operates at the highest speed in the frequency synthesizer and consumes a large portion of the power in the PD. In Fig.6 shows the block diagram of the modified DMP (16/17) prescaler typically consists of a divide-by-4/5 synchronous core, a divide-by-4 asynchronous divider and a feedback logic section. The 4/5 MC signal controls how many DFFs the prescaler input signal must travel through and therefore determines the division ratio. When the 4/5 MC is held low, the core always divides the input signal by 4 which then travels through asynchronous divide-by-4 circuit, resulting in a total division ratio of 16. If the 4/5 MC signal is high, the core will divide by 5. If feedback is produced such that the core is modulated to divide-by-5 once and by 4 three times the resulting division ratio is 17.

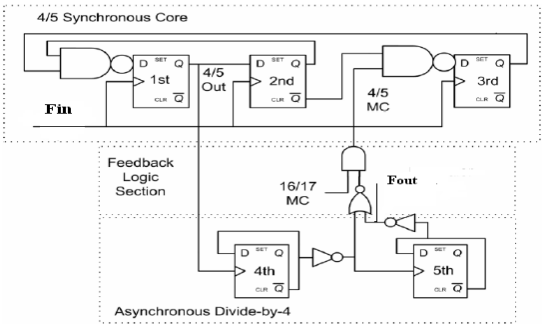

Fig.7 Block Diagram of DMP

A. Design of True Single Phase Clock (TSPC) FF. The TSPC DFF is generally known to consume less power than the common source logic (CSL) DFF because of there being no static DC currents.

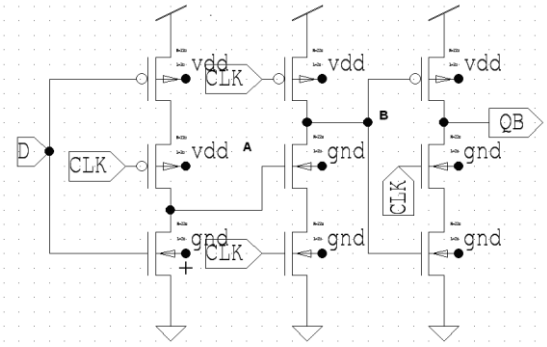

Fig.8 Schematic Diagram of TSPC DFF

When the DMP is implemented using a conventional TSPC DFF .The internal node B of the DFF is pre-charged and discharged with clock transitions, therefore the unnecessary toggling generates glitches on its internal stage when the input D value keeps low. In other words, when D keeps low and clk runs continuously then node A stays high which makes the M1 set to 'on' state. Then, the middle-stage gate functions as an inverter and generates glitches on node

B, which dissipate unwanted power consumption.

B. Design of Glitch less D-FF

The proposed glitch less DFF is given in the figure 9 and added clk generator for data-dependent pre-charge is shown in the figure 10. When input D stays low, the clk signal remains high and removes the

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charge-and-discharge operation at node B. This additional circuit occupies a small area and consumes only a negligible portion of DFF power since the switching activities of the D and A nodes are very low when compared to that of clk.

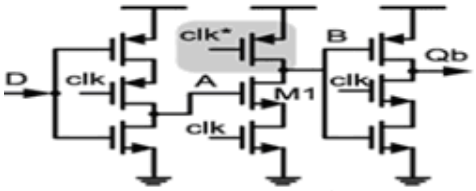

Fig. 9 Glitch less DFF

Although, the capacitive load on the clock path increases because of the added clk generator, since the proposed DMP uses only one glitch less DFF as DFF3.

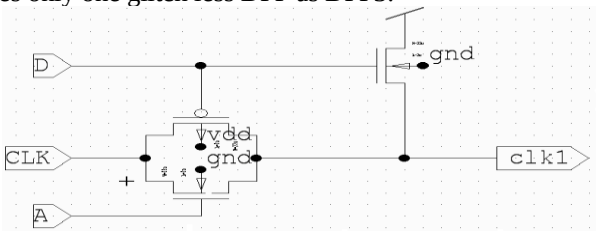

Fig.10 Added ClkGenerator For Data-Dependant Pre-Charge Suppression.

TABLE 1

VI. COMPARISON TABLE

Divider Circuit used	Power comparison	Maximum Division ratio Obtained(D)	Delay
CONVENTIONAL PD	62.9mW	34	7.83
EFFICENT PD	43mW	34	4.28
MODIFIED PD	52mW	118	4.39

The table 1 shows the comparison of efficient PD and conventional PD. Conventional PD has two counter and consumes 38mW power and maximum dividing factor obtained 34.Efficient PD consumes only 24 mW and uses only one counter and maximum dividing factor obtained is 34.

VII. CONCLUSIONS

A low-power PD based on a shared UC with a small control circuit, is presented in this paper. The use of RMCS generator enabled the adaptation of only one counter instead of using two counters in conventional divider. A glitch less DFF is also proposed for more power savings. Experimental results show that the proposed PD consumes around 12mW less power than conventional dividers. The PD proposed in this paper can provide the low-power for multi-standard frequency synthesizers

VIII. ACKNOWLEDGMENT

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