A Report on Differential Delay Analysis for Bus Codec

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Abstract*— Design of portable consumer electronic devices such as mobile phones, video game and other embedded systems are increasingly demanding low power consumption to maximize the battery life, reduce weight and increase reliability. These types of power sensitive devices are equipped with microprocessors as the processing elements and memories as the storage units. With current complementary metal oxide semiconductor technology a large portion of power consumption is consumed as dynamic power. Bus encoding techniques for low power consumption have been studied in the last couple of decades. Which includes Frequent Value Encoding method, Bus Invert Coding method and Gray Encoding Method .But these techniques could not become the part of Computer architecture because data profile based analysis was not done and delay based analysis was not done. So these techniques are not compatible to incorporate in the computer architecture. The contribution of our work is to design a methodology for optimizing CMOS circuits to incorporate the bus codec techniques by doing the delay based analysis.

***Index Terms*— Bus encoding, Differential Delay, Glitches, Inertial Delay**

I. INTRODUCTION

The continuing decrease in the feature size and the corresponding increases in the chip density and operating frequency have made a power consumption a major concern in VLSI design.[1] Excessive power dissipation in integrated circuits discourage their use in portable systems. It also causes overheating, which degrades the performance and reduces chip lifetime. The growing need for portable communication devices and computing systems has increased the need for optimization of power consumption in a chip.[2] Overall , low power design is an essential technology in the semiconductor industry today. Simultaneously we also need to speed the critical paths of the circuits, while reducing it's power consumption. The contribution of this work is to design a methodology for optimizing CMOS circuits for minimum dynamic power consumption without a loss in speed and free of glitches.

Revised Manuscript Received on December , 2011.

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II. LITERATURE SURVEY

Low power design of digital circuits is an important aspect of today's mobile electronic systems. It is observed that the

dynamic power consumption of the circuit is minimized when the delay of each gate is equals or exceeds the differential path delay at it's inputs.[3] Under this condition all unnecessary power consuming transitions are suppressed. In addition the overall input to output circuit delay must stay within the specified performance limit. This method can be used to speed up the critical paths of the circuit. Power optimization techniques have been implemented in various levels of design. The optimization of power is achieved by eliminating unnecessary transitions. This can be done either by controlling the delay of the gates or by inserting delay buffers.

III. MOTIVATION

Since bus codec techniques could not become the part of computer architecture. The motivation of our work is to design a methodology to solve this problem. Modern digital circuits consist of logic gates implemented in the complementary metal oxide semiconductor (CMOS) technology. The time taken for a CMOS logic gate output to change after one or more inputs have changed is called the output delay of the gate. The maximum difference in the signal arrival times at different inputs of a multi input gate is called the differential delay.[4] For correct functioning of CMOS circuits, every gate in the circuit needs to have an output transition, at most once for every input change. But in reality, the gates transition more than once due to unequal arrival times of signals at their inputs. These extra transitions are called glitches and they consume power.[6] This dynamic power due to glitches in a CMOS circuit need to be eliminated. In this methodology we propose a technique for eliminating glitches .

IV. WHAT ARE GLITCH REDUCTION TECHNIQUES

There have been many different techniques proposed for elimination of glitches in circuits. A total elimination of glitches requires path delays to satisfy certain conditions at every gate.[7] This can be done by balancing the paths by inserting buffers along slow paths .Gate delay can be non-linear function of the sizes of transistor in the gate.

Hence there have been techniques that treat the gates as an equivalent inverter whose sizes are treated as variables(gate sizing) or the transistor sizes then the entire circuit are treated as variable(transistor sizing).Another set of techniques called linear programming(LP) techniques model the system as a linear program with constraints set up to obtain the desired conditions at every gate of the circuit, and to limit the overall delay.

V. WHAT ARE DELAY ELEMENTS

Delay elements are components inserted into a digital circuit that do not alter the signal value ,but deliver the same waveform at the output with some extra delay.[8] In certain applications such as clock skew optimization ,the timing of signals need to be manipulated such that the arrival times of certain signals are delayed by given amounts. In these cases buffers are added to delay the waveform and meet the timing requirements.

Following is the classes of the category of delay elements:

1. Buffer: A buffer is the simplest of the delay elements. It is a pair (in general, any even number) of cascaded inverters that do not alter the nature of the signal. The delay added by the buffer is the time taken for the current to charge (or discharge) the load capacitance. In some cases during design, delay needs to be inserted for better performance or for synchronization; this is achieved by the introduction of delay elements. Buffer as delay elements are simple and reliable but their problem is increased dynamic power. Buffers can be used for larger delays.

2.Transmission Gates: A CMOS transmission gate is a bidirectional switch consisting of a parallel connection of an nMOS and pMOS transistor which are controlled by complementary signals.

3. Voltage Controlled Delay Elements: Voltage controlled delay elements are able to control the delay of the elements during runtime

VI. WHY ARE BUFFERS NECESSARY

Let us consider the simple combinational circuit shown in Figure 1.1. All the gates have a nominal delay of 1 unit. The critical path delay is defined as :

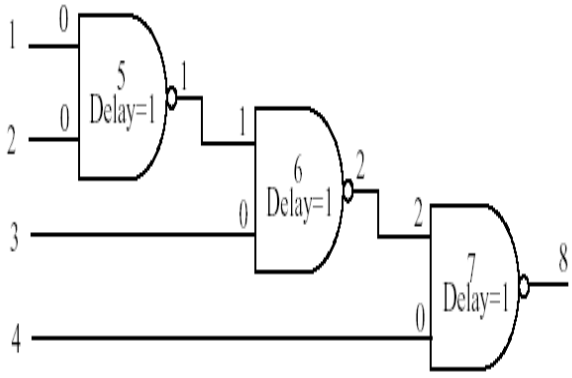

Figure 1.1. An example circuit with a critical path delay of 3 units. The gate delays and the arrival times of signals at the gate inputs are shown.

The delay of the slowest path through the circuit and it is 3 units in this case. The differential path delay is defined as the maximum difference of arrival times at the inputs of a gate. The inertial delay is the time taken by the gate output signal transition to occur after the input change causing the transition has occurred. The differential path delays of every gate are shown in figure 1.1.We need to optimize this circuit , such that the glitches are eliminated and the critical path delay is not increased. To prevent a gate from glitching the hazard filtering condition specifies that: Inertial delay of a gate >= Differential delay at gate inputs. [9] This condition needs to be satisfied by all gates in the circuit. In our example circuit of fig 1.1 we see that gate 7 does not satisfy this condition. If only hazard filtering is used for optimization The delay of gate 7 can be increased greater than the differential delay of 1 to satisfy the condition. Since the gate is on the critical path, we cannot increase it's delay.[10]

We can optimize the circuit by inserting a buffer at the input 4. The optimized circuit is shown in the Figure 1.2. The differential delays at the gate inputs after the buffer is inserted are shown in figure 1.2. The differential delay at gate 7 satisfies the hazard filtering condition as the input 4 is delayed by the buffer. Thus the circuit is glitch free and also works at the critical path delay of 3 units. The buffer was needed in this design because of the conventional gate design.[11] pg. No [105]

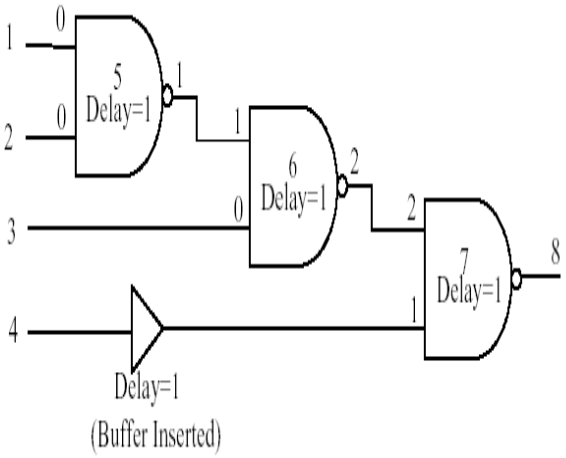

Fig 1.2 : The optimized circuit of Fig 1.1 the optimization is done by the insertion of delay buffer.

VII. RESULTS AND FINDINGS

Since the Bus Codec techniques are not compatible to incorporate .The problem is to find a glitch reduction technique that eliminates glitches in the circuit without any reduction in speed. The technique should be scalable to large circuits. Among the various glitch reduction techniques the buffer insertion technique can be realizable at the physical level of design.

VIII. CONCLUSION

It has been observed that bus encoding techniques were not followed by delay based analysis. Glitches are the power wastage in CMOS circuits and needs to be eliminated. The various glitch reduction techniques were presented. Then the various delay elements were discussed. The buffer insertion technique has been presented in detail, how it can be used for controlling the delay of the gates.

Buffer as delay elements are simple to use at design level. Because of their signal regenerative property they can be inserted in the circuit for larger delays to work with any load capacitance. Contribution of our work is to design a methodology for optimizing CMOS circuits for minimum dynamic power consumption without a loss in speed and free of glitches.

REFERENCES

1. Ji Gu,Hui Guo "An efficient segment bus invert coding method for instruction memory data bus switching reduction" in EURASIP journal on embedded systems vol. 2009.
2. M.R.Stan,W.P.Burleson "Bus Invert coding for low power I/O" IEEE transactions on VLSI systems,Vol 3,No 1,pp 49-58, 1995.
3. M.S.Elrabaa,I.S.Abu Khater,and M.I. Elmasry, "Advanced Low Power Digital CircuitsTechniques.Boston:Kluwer" Academic Publishers, 1997.
4. F.A. Najm, " A Survey of power estimation techniques in VLSI circuits".IEEE transactions on VLSI systems, vol 2,NO.4.pp 446 -455, 1994.
5. T. Raja,V.D.Agrawal,M.L. Bushnell, "Variable input delay CMOS logic for low power design" in proc. 18 th international conference on VLSI design, pp 596-604, 2005.
6. Yuanlin Lu,V.D.Agrawal, "CMOS leakage and glitch minimization for power performance tradeoff " in journal of low power electronics Vol-2 ,pp 1-10,2006.
7. T. Raja,V.D.Agrawal,M.L. Bushnell, " Transister sizing of logic gates to maximize input delay variability " in journal of low power electronics Vol-2,pp 121-128,2006.
8. N.Mahapatra,A .Tareen and S.V.Garimella " Comparison and Analysis of Delay Elements" in proc. of IEEE Computer Society Annual Workshop on VLSI , pp 81-86, 2000.
9. T. Raja,V.D.Agrawal,M.L. Bushnell, " Design of variable input delay gates for low dynamic power circuits " . in Proc. the international workshop on power and timing modeling, optimization and simulation, pp 436-445,2005.
10. V.D.Agrawal, " Low power design by hazard filtering " in proc. Of international conference on VLSI design , pp 193-197,1997 .
11. Tezaswi Raja " Minimum dynamic power CMOS design with variable input delay logic".