

# Distributed Routing Simulation for Generic Network-on-Chip Topologies

Naveen Choudhary

**Abstract:** Networks-on-Chip (NoC) is recently proposed as an alternative to the on-chip bus to meet the increasing requirement of complex communication needs in Systems-on-Chip (SoC). Most researchers advocate the use of traditional regular networks like meshes as architectural templates which gained a high popularity in general-purpose parallel computing. However, most SoC platforms are special-purpose tailored to the domain-specific requirements of their application. They are usually built from a large diversity of heterogeneous components which communicate in a very specific, mostly irregular way. In such systems the size and nature of cores may vary quite widely making the topology irregular. Moreover regular topologies can become irregular due to faults in links and switches. In such scenario topology agnostic routing algorithms are generally required. In this paper, we have analyzed the performance and applicability distributed table based routing for irregular NoC on an Network-on-Chip simulation framework.

**Index Terms:** Distributed routing, Interconnection networks, NoC, SoC.

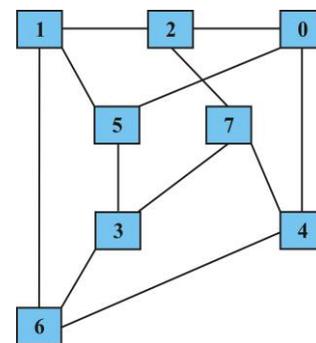
## I. INTRODUCTION

Ever since the innovation of the integrated circuit in the 1960's, the number of transistors available on one chip has increased with approximately 60 percent a year and with these continual developments of technology, communication between various ICs has also increased day by day. According to ITRS [1], the realization of complex Systems on a Chip (SoCs) consisting of billions of transistors fabricated in technologies characterized by 32 nm feature size and less will soon be feasible. Such SoCs imply the seamless integration of numerous IPs like DSP and FPGA performing different functions and operating at different clock frequencies. The integration of several homogenous or heterogeneous components into a single system gives rise to new challenges. With the change of dramatic improvement in this area it is essential to have an adaptable communication facility that can cope up with the versatile programming of the cores. To achieve the above-mentioned requirements the use of a network-centric approach i.e. Network on Chip (NoC) [2], [3] is a promising way. To meet the challenge of large scale chip integrity, on-chip communication is playing an increasingly dominant role in System-on-Chip (SoC) design. Assuming the complexities of futuristic embedded processors, several hundreds or even thousands of embedded

processors can fit on a single chip. These designs typically show a high degree of modularity and inherent computational parallelism. This trend is accompanied by revolutionary changes of the employed design methodology where a paradigm shift from a computation-centric view to a communication-centric becomes evident [2], [3].

Fig. 1. Application Specific Irregular Network-on-Chip

Functionality of such systems is often captured by a set of communicating tasks at a high level of abstraction. These are mapped to computational resources which are then interconnected by a central communication backbone. The



efficiency of the overall design is governed by this communication architecture which plays a key role in modern SoC platforms. It impacts both performance and implementation costs in terms of silicon area and energy consumption to a substantial extent. Some of the most important phases in designing the NoC are the design of the topology or structure of the network and setting of various design parameters (such as frequency of operation, link-width, etc). Several early works [2], [3] favored the use of standard topologies such as meshes, tori, under the assumption of modular design and also the wires can be well structured in such topologies. However, most SoCs are heterogeneous, with each core having different size, functionality and communication requirements. Thus, standard topologies can have a structure that poorly matches application traffic. An application specific irregular topology is shown in Figure 1. In addition to above mentioned applicability of irregular topologies in application specific NoCs, the generic regular topologies can also become irregular for supporting oversized region [4], [5] or due to faults in switches or links in the regular NoCs.

If the topology is regular, it is wise with regards to performance, to use a topology dependent routing since it would be able to exploit the regularity of the topology. Dimension-Order Routing (DOR/XY) [6] and odd-even routing are such algorithms suitable for meshes. Unfortunately, these algorithms are sensitive to topology

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changes. A faulty switch or link will degrade the topology into an irregular one and then the algorithms will fail.

A simple way to achieve fault-tolerance is by the use of a topology agnostic routing algorithm may be in the combination with *static* reconfiguration if required. Generally the topology agnostic routing function proposed in the NoC research domain fall in the category of table based distributed routing. Prominent examples of such table based deadlock free distributed routing functions for irregular NoC include up\*/down\* [7], lturn [8], down/up [9], and prefix-routing [10]. These algorithms have in common that they are based on turn prohibition [11] and require a route mapping table in each router.

This paper analyzes the application of distributed table based routing function in irregular NoC and presents an experimental comparison with their regular counterparts. The rest of the paper is organized as follow. In section 2 we survey the basic communication architecture and issues pertaining to NoC. Section 3 presents a brief introduction to issues in table based distributed routing. The functionality of up\*/down\* routing is presented in detail to highlight the issue pertaining to distributed table based routing for Irregular NoC. Section 4 analyzes the performance of distributed table based routing for irregular NoC with the help of a NoC performance simulator. In this section comparative performance result of distributed table based routing for irregular NoC in comparison with the standard routing function for 2D-Mesh based NoC are also presented. In section 4 we conclude.

### II. NOC ARCHITECTURE AND DESIGN CHALLENGES

Chip design has four distinct aspects: computation, memory, communication, and I/O. As processing power has increased and data intensive applications have emerged, the challenge of the communication aspect in single-chip systems, Systems-on-Chip (SoC), has attracted increasing attention. A prominent concept for communication in SoC is known as Network-on-Chip (NoC). NoC does not constitute an explicit new alternative for intra-chip communication but is rather a concept which presents a unification of on-chip communication solutions. In this section, we briefly introduce some basic NoC issues.

#### A. Topology

The topology of a NoC specifies the physical organization of the interconnection network. It defines how nodes, switches and links are connected to each other. Topologies for NoCs can be classified into two broad categories: 1) direct network topologies, in which each node (switch) is connected to at least one core, and 2) indirect network topologies, in which we have a subset of switches (nodes) not connected to any core and performing only network operation. Both the topology mentioned above can be regular like meshes, tori, k-ary n-cubes and fat trees or irregular customized application-specific topology.

#### B. Routing Function

Routing is the process of selecting paths in the computer network, along which data or physical traffic is sent. Routing algorithms are responsible for correctly and efficiently routing packets or circuits from the source to destination [2]. Routing schemes are usually categorized into two folds: deterministic routing and adaptive routing. Deterministic routing means routing paths are completely determined statically and the packets follow the same path for a given source-destination pair, while in adaptive routing, the paths are determined dynamically depending on network

congestion conditions. Deterministic routing has the design simplicity and low latency under low network traffic, but performance throughput degrades when there is network congestion. Adaptive routing uses alternative paths when network is congested, which provides higher throughput, although it will experience higher latency if network congestion is low. In NoCs, the routing scheme usually selects candidates among the routing paths that have minimum distance between the source and destination nodes. There are many routing algorithms available e.g. XY routing [12] and odd-even routing [13] are the popular routing functions for 2D-Mesh regular NoC. They are both theoretically guaranteed to be free of deadlock and livelock. The XY routing strategy can be applied to regular two-dimensional mesh topologies without obstacles. The position of the mesh nodes and their nested network components is described by coordinates, the x-coordinate for the horizontal and the y-coordinate for the vertical position. A packet is routed to the correct horizontal position first and then in vertical direction. XY routing produces minimal paths without redundancy, assuming that the network description of a mesh node does not define redundancy. The odd-even turn model is a shortest path routing algorithm that restricts the locations where some types of turns can take place such that the algorithm remains deadlock-free. More precisely, the odd-even routing prohibits the *east to north* and *east to south* turns at any tiles located in an even column. It also prohibits the *north to west* and *south to west* turns at any tiles located in an odd column. Similarly are many routing function to support irregular NoC. A brief explanation of issues in distributed table based routing function for irregular NoC are explained in Section 3.

#### C. Switching Scheme

The NoC switching strategy determines how data flows through the routers in the networks. It defines the granularity of data transfer and the switching technique. NoCs use packet switching as the fundamental transportation mode. Packet switching is a communications paradigm in which packets (discrete blocks of data) are routed between nodes over data links shared with other traffic. In each network node, packets are queued or buffered, resulting in variable delay. This contrasts with the other principal paradigm, circuit switching, which sets up a limited number of constant bit rate and constant delay connections between nodes for their exclusive use for the duration of the communication. In packet switching, instead of establishing a path before sending any data, the packets are transmitted from the source and make their way independently to the receiver, possibly along different routes and with different delays. There are mainly three kinds of packet switching schemes [12]: store-and-forward, virtual cut-through and wormhole switching.

**Store-and-forward** is a telecommunications technique in which information is sent to an intermediate station where it is kept and sent at a later time to the final destination or to another intermediate station.

The intermediate station (switch) or node forwards the bits of the packet only when the entire packet is received by it.

**Virtual cut-through** switching is a switching method for packet switching systems, wherein the intermediate switch

starts forwarding a frame (or packet) before the whole frame has been received if there is ample space for the whole packet in the later switch (switch where the packet is being forwarded), normally as soon as the destination address is processed. This technique reduces latency through the switch, but decreases reliability. **Wormhole switching** combines packet switching with the data streaming quality of circuit switching to attain minimal packet latency. The node looks at the header of the packet to determine its next hop and immediately forwards it. The subsequent flits are forwarded as they arrive. This causes the packet to *worm* its way through the network, possibly spanning a number of nodes, hence the name. The latency within the router is not that of the whole packet. A stalling packet, however, has the unpleasant expensive side effect of occupying all the links that the worm spans. Because of the limited silicon resources and the low-latency requirements for typical NoC applications, most NoC architectures use Wormhole switching scheme for the on-chip routers. In this paper, the wormhole switching is assumed for the experimental results.

D. NoC Communication Energy Model

As the characteristic of NoC, power dissipation is a critical issue of the NoC design. We only consider communication power dissipation which is consumed on the router. Most researchers use power modeling with bit energy, which is the power consumption of transferring a bit of data from the source node to the destination, as the energy model of NoC. The power is mainly consumed by three sources: the internal node switches, the internal buffer queues and the interconnect wires [14, 15]. The degree of switch power consumption is decided by the choices of process technologies, voltage levels and operating frequencies. The internal buffer power consumption mainly comes from the occurrences of destination contentions and interconnects contentions in the buffer memories. The interconnect wires power consumption is directly related to the link lengths.

E. Flow Control

Flow control mainly addresses the issue of ensuring correct operation of the network. In addition, it can be extended to also include issues on utilizing network resources optimally and providing predictable performance of communication services. In the following, first the concept of virtual channels [12] and their use in flow control is discussed and later buffering issues are briefly discussed. Virtual channels (VCs): VCs are the sharing of a physical channel by several logically separate channels with individual and independent buffer queues. Generally 2 to 16 VCs per physical channel have been proposed for NoCs. Their implementation results in an area and possibly also power and latency overhead due to the cost of control and buffer implementation. There are however a number of advantageous of using VCs as shown below.

- **Avoiding Deadlocks:** Since VCs are not mutually dependent on each other, by adding VCs to links and choosing the routing scheme properly, one may break cycles in the resource dependency graph [16] and thus deadlocks can be avoided.
- **Optimizing Wire Utilization:** In future technologies, wire costs are projected to dominate over transistor costs. Letting several logical channels share the physical wires, the wire utilization can be greatly

increased. Advantages include reduced leakage power and wire routing congestion.

- **Improving Performance:** VCs can generally be used to relax the inter-resource dependencies in the network, thus minimizing the frequency of stalls. In Dally [17], it is shown that dividing a fixed buffer size across a number of VCs improve the network performance at high loads. In Duato and Pinkston [18], the use of VCs to implement adaptive routing protocols is presented. Vaidya et al. [19] and Cole et al. [20] discusses the impact and benefit of supporting VCs.
- **Providing QoS Services :** Quality-of-service (QoS) can be used as a tool to optimize application performance. VCs can be used to implement such services by allowing high priority data streams to overtake those of lower priority [21] or by providing guaranteed service levels on dedicated connections [22].

III. DISTRIBUTED ROUTING FOR IRREGULAR NOC

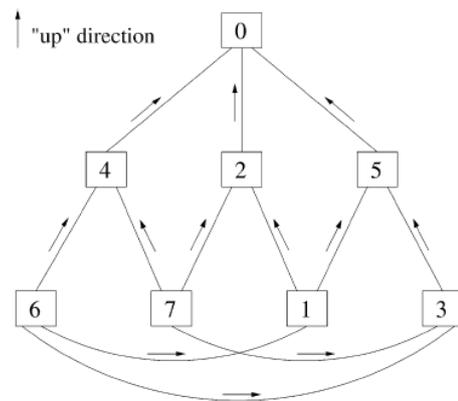


Fig. 2. Tree based topology representation of irregular NoC in Figure 1.

*Up\*/down\** [7] routing algorithm is distributed in nature, and is implemented using table-look-up. The routing table in each switch must be established before data packets can be routed. To do so, a breadth-first spanning tree (BFS) on the *Interconnection topology graph N* is computed. *Up\*/down\** routing is based on an assignment of direction to the operational links/channels, including the ones that do not belong to the tree. In particular, the “up” of each link is defined as end connected to 1) the router node which is closer to the root in the spanning tree or 2) the router node with lower ID, if both ends are connected to router nodes at the same tree level. Links looped back to the same router node are omitted from the configuration. The result of this assignment is that each cycle in the network has at least one link in the “up” direction and one link in the “down” direction. Figure 2 is the tree representation of the irregular NoC exhibited in Figure 1.

To eliminate deadlocks

in *up\*/down\** routing, a legal route must traverse zero or more links in the “up” direction followed by zero or more links in the “down” direction. Thus, cyclic dependencies between channels



are avoided because a message cannot traverse a link along the “up” direction after having traversed one in the “down” direction. Such routing not only guarantees deadlock-freedom, but also provides adaptivity owing to existence of multiple valid paths using “up/down” rule. The route look-up tables can be constructed to support both minimal and non-minimal adaptive routing [6]. Minimal routing usually provides better performance because messages occupy fewer resources on average. However, in some cases, up\*/down\* routing may not be able to supply any minimal path between some pairs of switches. In [23] Silla et.

al proposed general methodologies for the design of adaptive routing algorithms for networks with irregular topology. Routing algorithms designed according to these methodologies allows messages to follow minimal paths in most cases, reducing message latency and increasing network throughput. Given an interconnection network and a deadlock-free routing function defined on it, it is possible to duplicate all the physical channels in the network, taking advantage of spare switch ports or by splitting the physical channels into two virtual channels. In both cases, the graph

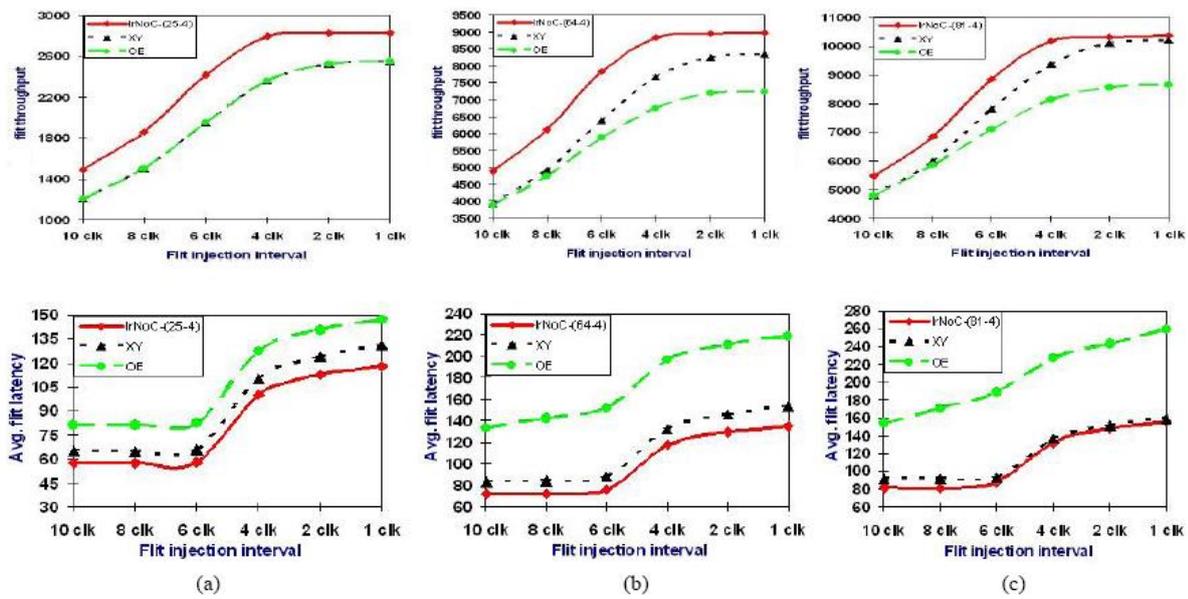


Fig. 3. Performance comparison of various instance different size customized irregular NoC topologies (IrNoC) with corresponding same sized 2-D Mesh topology with X-Y and OE routing with varying packet injection interval (a) NoC with no. of Cores = 25, (b) NoC with no. of Cores = 64 , (c) NoC with no. of Cores = 81

representation of the network contains the original and the new channels. Silla et. al. [23] then propose to extend the routing function in such a way that newly injected messages can use new channels without any restriction as long as the original channels are used exactly in the same way as in the original routing function. In this paper original channels are made to use up\*/down\* deadlock free routing function and new channels are allowed to follow the shortest available path to the destination. The modified routing function allows a packet arriving on a new channel following shortest path to be routed to any channel without any restrictions but preferably with higher priority to new channels as new channel assures shorter paths and higher adaptively (flexibility) . If no new channels are available due to congestion one of the original channels following up\*/down\* must be provided. However, once a packet acquires an original channel following up\*/down\* path, it is not allowed to do transition to a new channel anymore to avoid deadlock situation. Moreover to increase adaptivity and to ensure that most packets follow the minimal path, the new packet entering the network can only leave the source switch by using the new channels that provide a minimal path toward the destination.

I. EXPERIMENTAL RESULTS

A. NoC Performance Simulation Framework

A discrete event, cycle accurate simulator called IrNIRGAM [24] is used for customized Irregular NoC. IrNIRGAM is an extension of NIRGAM [25]. NIRAGM is a cycle-accurate SystemC based simulator for regular NoC. IrNIRGAM supports irregular topology framework with source and table based distributed routing. For IrNIRGAM a wormhole switching based network architecture is implemented, where an IP Core directly connected to a dedicated router, is assumed (Direct Network). In general, the topology represents the most important characteristic of NoC architectures. It defines how router nodes are physically interconnected and has a predominant influence on network performance and implementation costs.

In IrNIRGAM, input buffered routers can have multiple virtual channels (VCs) and uses wormhole switching for flow control. The packets are split into an arbitrary number of flits (flow control units) and forwarded



through the network in a pipelined fashion. A Round-Robin scheme for switch arbitration is used in the router nodes to provide fair bandwidth allocation while effectively preventing scheduling anomalies like starvation.

For performance comparison *IrNIRGAM* was run for 10000 clock cycles and network throughput in flits and average flit latency were used as parameters for comparison. Network throughput is the number of flits received by various cores of the NoC during the simulation run. The flit latency determines the number of clock cycles it takes from entering the network until the reception at the target node. It is worth mentioning that these latency values do not include the source queuing time i.e. time period a flit waits at the source node in case of a congested out-channel. Therefore, latency and throughput are expected to saturate towards high injection load of flits. All data queues in the network routers can buffer eight flits per channel.

**B. Up\*/down\*, X-Y and O-E Routing Function Performance Comparison**

Figure 3 shows the performance comparison of various instances of different sized customized Irregular NoC with up\*/down\* routing (*IrNoC*) with corresponding similar sized 2-D Mesh topology with X-Y and OE routing with varying packet injection interval. *IrNoC* with up\*/down\* routing function consistently showed significantly improved throughput in flits at reasonably lesser average flit latency in comparison to regular 2D-mesh NoC with XY and OE routing.

Figure 4 summarizes the performance results averaged over 50 irregular topologies (*IrNoC*) using distributed table based up\*/down\* routing function with permitted node/core degree of 6 and 4 with number of cores varying between 16 to 81 and 2D-mesh of equal number of cores as in *IrNoC* with XY and OE (odd-even) routing.

Figure 4 show that *IrNoCs* sustain a higher flit throughput and lower transmission latency in all cases. *IrNoC* with permitted node degree of 6 achieves 19.4% and 32% more flit throughput on average with decrease in average flit latency of 15.3 and 60.3 clock cycles in comparison to corresponding 2D-mesh with XY and OE routing respectively. Similarly *IrNoC* with permitted node degree of 4 achieves 7.6% and 19% more throughput on average with decrease in average flit latency of 12.6 and 57.6 clock cycles in comparison to corresponding 2-D Mesh with X-Y and OE routing respectively.

Figure 5 shows throughput in flits and latency comparison of *IrNoC* (with permitted node degree of 4 & 6) and 2-D mesh with X-Y and OE routing with varying flit injection interval in clock cycles.

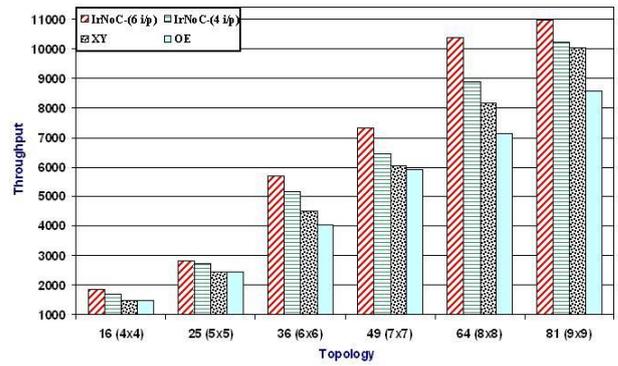
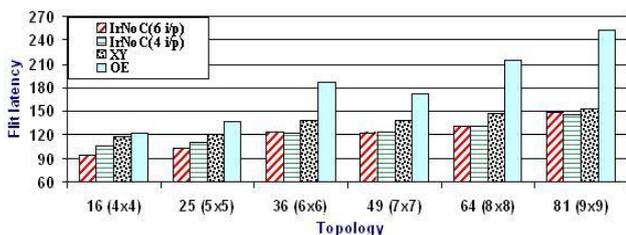


Fig. 4. Average performance comparison of *IrNoC* with 2-D Mesh topology with X-Y and OE routing

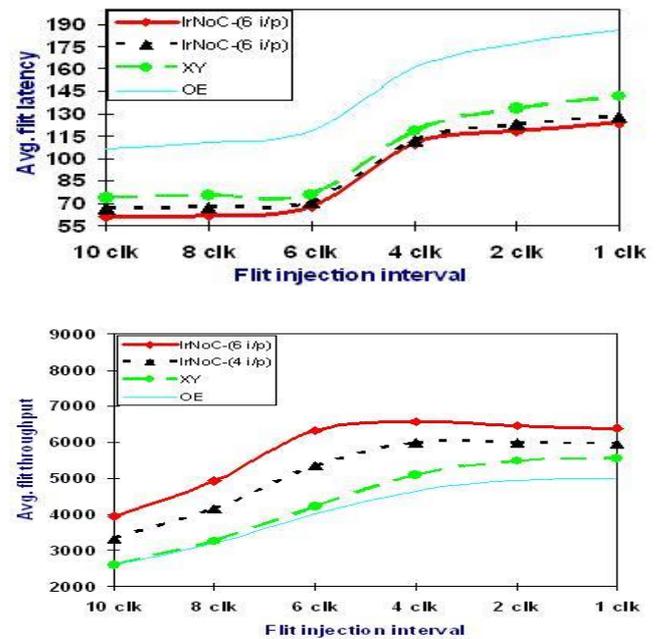


Fig. 5. Average performance comparison of *IrNoC* with 2-D Mesh topology with X-Y and OE routing with varying flit injection interval

Figure 5 shows that the *IrNoC* with distributed up\*/down\* routing consistently shows better performance in comparison with the regular 2D-Mesh NoC with X-Y and O-E routing function.

**II. CONCLUSION**

The paper analyzes the application of distributed table based routing function in irregular NoC and presents an experimental comparison with their regular counterparts. The paper shows with the help of experimental results that for the application customized Irregular NoC the distributed table based routing can outperform routing function such as X-Y and OE for standard regular NoC such as 2D-Mesh. However distributed table based routing puts an extra overhead in terms space on each router and this need to be optimized and further research can be undertaken in the



NoC research domain to find an appropriate representation of such table in the router such that table space can be minimized without compromising the efficiency of the routing function.

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