Designing & FPGA Implementation of IIR Filter Used for detecting clinical information from ECG

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Abstract: This paper describes an approach to design and implementation of digital filter algorthims based on field programmable gate arrays (FPGAs).The advantages of FPGA approach to digital filter implementation include higher sampling rates than are available from traditional DSP chips, lower cost than ASIC for moderate volume applications An ECG is a simple and useful test which records the rhythm and electrical activity of the heart of the patient that suffers from any heart disease

While recording ECG signal it gets corrupted due to different noise interferences and artefacts. Noise and interference are usually large enough to obscure small amplitude features of the ECG hat are of physiological or clinical interest. The bandwidth of the noise overlaps that of wanted signals, so that simple filtering cannot sufficiently enhance the signal to noise ratio...We have used MATLAB for this purpose as it is the most advanced tool for DSP applications. Also it helps to verify the design and results that comes from the hardware.

Keywords: *FIR, IIR, FPGA,Mat lab, VHDL.*

I Introduction

Electrocardiogram (ECG) is one of the most important electrical signals in the field of medical science which has a great need to be processed before further analysis. There are various methods to remove the noise of the ECG signal which may involve the IIR or FIR filter. Each has its own advantages and disadvantages. FIR filter because of its finite impulse response is always stable but its number of coefficients is very large, so it needs a larger memory space to store its cofficents. On the other hand the IIR filter has less number of coefficients and can be unstable sometimes due feedback loop involved in it. Essentially, Equation for FIR filtering is a 1-D convolution between the filter coefficients and the input data. In performing convolution, one of the two sets of numbers is reversed and "slid past" the other.

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The resulting stream of numbers is found by taking the sum of the multiplications at each sliding interval. Like the IIR structure, The FIR realization can be highly replica table, which becomes important in the hardware design. One important aspect of FIRs is the linear phase characteristic, which makes it ideal for most digital signal processing applications [1, 2]. Achieve the smaller side lobes in the stop band of. Despite the higher order of the FIR filter, the implementation is feasible in hardware and possesses the necessary linear phase property needed by channel models .Filter properties, design criteria, and the applications are the important parameters used to decide which filter to choose.

II Designing Process of IIR Filter

The Digital Filter Design problem involves the determination of a set of filter coefficients to meet a set of design specifications. These specifications typically consist of the width of the pass band and the corresponding gain, the width of the stop band(s) and the attenuation therein; the band edge frequencies (which give an indication of the transition band) and the peak ripple tolerable in the pass band and stop band(s).Plainly the IIR filter is not difficult to understand. An ECG waveform has been shown below before and after addition of baseline and power line noise
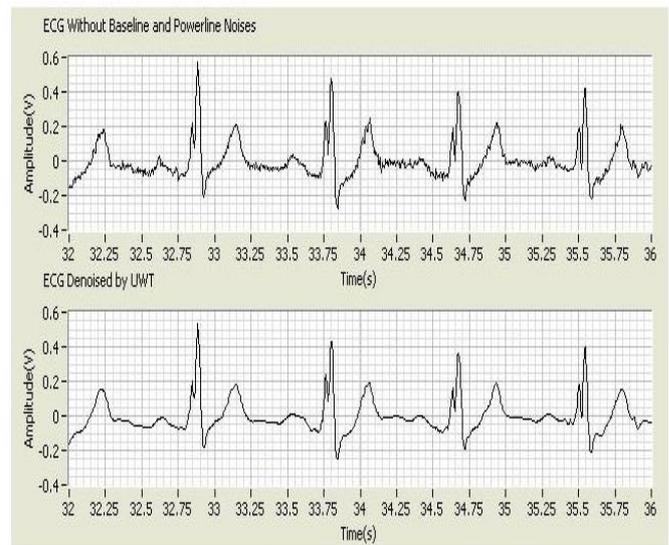

Figure1: ECG waveform before and after Noise

We take a set of samples a fixed time apart, and multiply them by a set of coefficients.

This has an effect on the signal; by varying the coefficients we can choose what the filter does [3, 4].

The combination of the length of the filter (number of taps) and the values of the coefficients determine the filter's operation. Designing the filter is just a case of deciding how many taps and choosing the coefficients. There are many techniques for selecting coefficients. Architecture of IIR filter used has been shown below. The various blocks used in architecture of Digital IIR filter are multipliers, adders, flip flops have been shown below.

Figure 2: Architecture of IIR filter

In the project I have used the Parks-McClellan Algorithm to calculate the coefficients. This algorithm gives the minimum order Filter for the given specifications. The filter thus designed is Equiripple Linear phase IIR filter. To calculate each output of the IIR filter, we multiply a set of samples by a set of coefficients. When a new sample arrives, it is added to the sample set, and the oldest sample is disposed of. This can be performed using the circular addressing hardware [5, 6, and 7].

Steps Involved in Designing IIR Filter

1. Filter Specification
2. Find filter coefficients that meet the specification
3. Calculation of Coefficient quantization and quantization noise effects
4. Realization of filter structure (Direct Form, Transposed Form, Cascade, or Lattice)

The computational algorithm implementing equation of an IIR filter can be conveniently represented in block diagram. It is done using building blocks elements such as Multipliers, Adders and the Delays. This way of presenting the difference equations in the form of block diagram and Signal Flow Diagram makes easy to write an algorithm,

which can be implemented in the digital computer. Comparison of both filters has been shown below.

Filter	Order of filter	No. of adders	No. of multipliers	No. of delays
FIR	450	450	451	450
IIR	2	4	4	2

As it is clear from comparison, no of adders, multipliers are very less in IIR as compare to FIR. Another comparison has been done on basis of structure used for IIR filter. Following table shows comparisons of various structures which can be used for implementation of IIR filter.

Structure	Number of multiplications	Number of additions and subtractions	Total number of operations	Required bitwidth
Direct form	16	16	40	21
Cascade	13	16	34	12
Parallel	18	16	39	11
Continued fraction	18	16	35	23
Ladder	17	32	50	14
Wave digital	11	30	47	12

As it is clear that Cascade form requires very less no of total operators... A typical ECG waveform has been shown in figure.

A typical ECG Waveform

III FPGA Implementation

Although not new to the realm of programmable devices, field programmable gate arrays (FPGAs) are becoming increasingly popular for rapid prototyping of designs with the aid of software simulation and synthesis.

Software synthesis tools translate high-level language descriptions of the implementation into formats that may be loaded directly into the FPGAs.

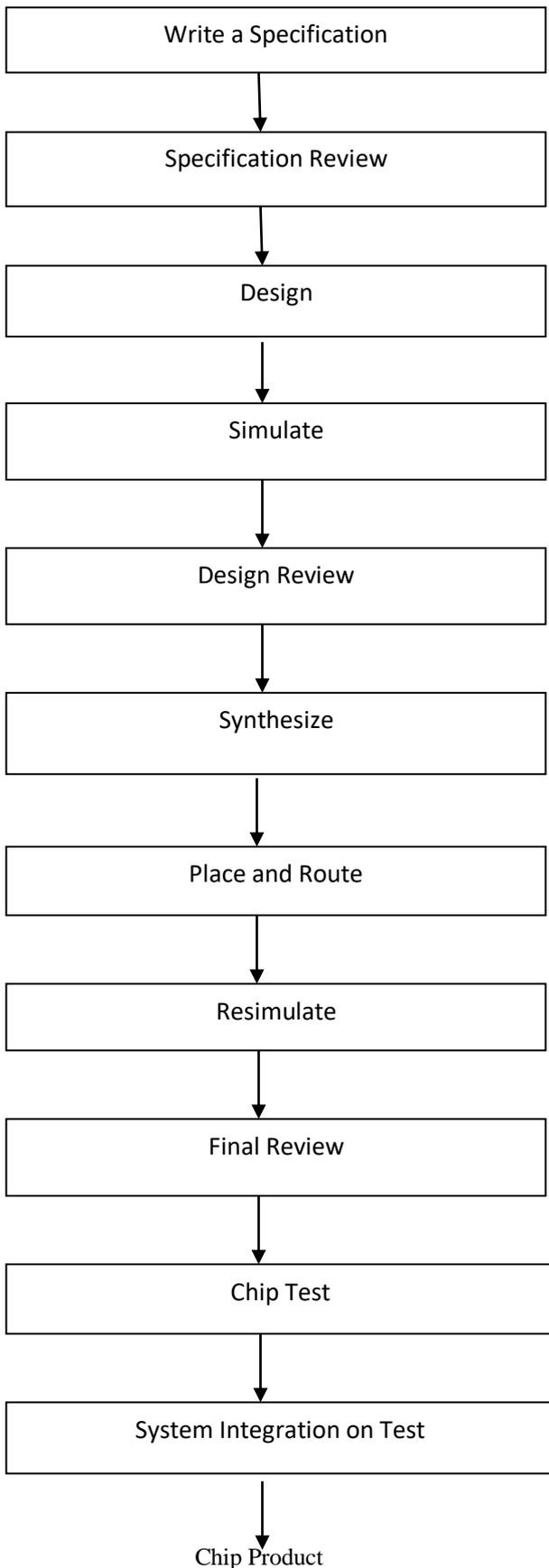An increasing number of design changes through software synthesis become more cost

Write a Specification

Specification Review

Design

Simulate

Design Review

Synthesize

Place and Route

Resimulate

Final Review

Chip Test

System Integration on Test

Chip Product

Figure 3 FPGA Design Flow

effective than similar changes done for hardware prototypes. In addition, the implementation may be constructed on existing hardware to help further reduce the cost [8, 9].

This the entire process for designing a device that guarantees that you will not overlook any steps and that you will have the best chance of getting backs a working prototype that functions correctly in your system. The design flow consists of the steps in:

Step 1: Writing a Specification

The importance of a specification cannot be overstated. This is an absolute must, especially as a guide for choosing the right technology and for making your needs known to the vendor. As specification allows each engineer to understand the entire design and his or her piece of it. It allows the engineer to design the correct interface to the rest of the pieces of the chip. It also saves time and misunderstanding. There is no excuse for not having a specification.

A specification should include the following information:

- An external block diagram showing how the chip fits into the system.
- An internal block diagram showing each major functional section.
- A description of the I/ pins including
- Output drive capability
- Input estimates including
- Timing estimates including
- Setup and hold times for input pins
- Propagation times for output pins.
- Clock cycle time
- Estimated gate count
- Package type

It is also very important to understand that this is a living document. Many sections will have best guesses in them, but these will change as the chip is being designed.

Step 2: Choosing a Technology

Once a specification has been written, it can be used to find the best vendor with a technology and price structure that best meets your requirements.

Step 3: Choosing a Design Entry Method

One must decide at this point which design entry method you prefer. For smaller chips, schematic entry is often the method of choice, especially if the design engineer is already familiar with the tools. For larger designs, however, a hardware description language (HDL) such as Verilog or VHDL is used because of its portability, flexibility, and readability. When using a high level language, synthesis software will be required to "synthesize" the design. This means that the software create slow level gates from the high level description.

Step 4: Choosing a Synthesis Tool

One must decide at this point which synthesis software you will be using if you plan to design the FPGA with an HDL.

This is important since each synthesis tool has recommended or mandatory methods of designing hardware so that it can correctly perform synthesis. It will be necessary to know these methods up front so that sections of the chip will not need to be redesigned later on. At the end of this phase it is very important to have a design review. All appropriate personnel should review the decisions to be certain that the specification is correct, and that the correct technology and design entry method have been chosen.
Step 5: Designing the chip

It is very important to follow good design practices. This means taking into account the following design issues.

Step 6: Simulating- Design Review

Simulation is an ongoing process while the design is being done. Small sections of the design should be simulated separately before hooking them up to larger sections. There will be much iteration of design and simulation in order to get the correct functionality. Once design and simulation are finished, another design review must take place so that the design can be checked. It is important to get others to look over the simulations and make sure that nothing was missed and that no improper assumption was made. This is one of the most important reviews because it is only with correct and complete simulation that you will know that your chip will work correctly in your system.

Step 7: Synthesis

If the design was entered using an HDL, the next step is to synthesize the chip. This involves using synthesis software to optimally translate your register transfer level (RTL) design into a gate level design that can be mapped to logic blocks in the FPGA. This may involve specifying switches and optimization criteria in the HDL code, or playing with parameters of the synthesis software in order to insure good timing and utilization.

Step 8: Place and Route

The next step is to lay out the chip, resulting in a real physical design for a real chip. This involves using the vendor's software tools to optimize the programming of the chip to implement the design. Then the design is programmed into the chip.

Step 9: Resituating – Final Review

After layout, the chip must be resituated with the new timing numbers produced by the actual layout. If everything has gone well up to this point, the new simulation results will agree with the predicted results. Otherwise, there are three possible paths to go in the design flow. If the problems encountered here are significant, sections of the FPGA may need to be redesigned. If there are simply some marginal timing paths or the design is slightly larger than the FPGA, it may be necessary to perform another synthesis with better constraints or simply another place and route with better constraints. At this point, a final review is necessary to confirm that nothing has been overlooked.

Step 10: Testing

For a programmable device, we have to simply program the device and immediately have your prototypes. You then have the responsibility to place these prototypes in your system and determine that the entire system actually works

correctly. If you have followed the procedure up to this point, chances are very good that your system will perform correctly with only minor problems. These problems can often be worked around by modifying the system or changing the system software. These problems need to be tested and documented so that they can be fixed on the next revision of the chip.

However, it is possible to replace a general purpose DSP chip and design special hardware digital filters which will operate at video-speed sampling rates. In other cases, the speed limitations can be overcome by first storing the high speed ADC data in a buffer memory. The buffer memory is then read at a rate which is compatible with the speed of the DSP-based digital filter.

IV   Conclusion

By observing the VHDL simulation results of IIR and FIR filters we conclude that both the filters perform their filtering functions correctly which matches the MATLAB design of the filters. Low pass IIR filter gave the correct pre-synthesis and post-synthesis simulation results and requires less memory on FPGA kit as comparison to FIR Post place and route simulation was used to find the actual delays caused by the hardware implementation of the IIR filter on FPGA. We found that the delay between FSCLK and MCLK is 6.5 ns and delay between input and output signal is 998396.5 ns.

V   Results & Waveforms

We have designed the filter first in MATLAB in order to check the feasibility of the specifications in MATLAB. We get the desired results in MATLAB. Then the filter with the desired specifications was designed in VHDL and simulated in Modelsim software and after that burned on FPGA kit.
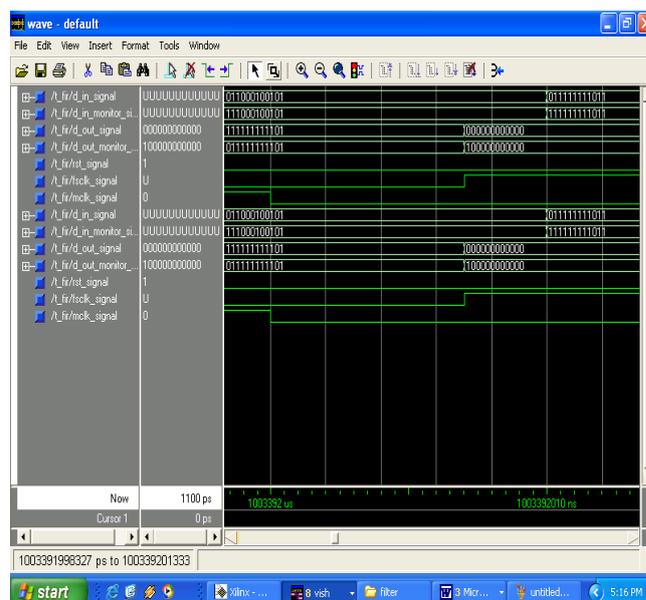

Figure 4: Modelsim Output.

The VHDL code of the digital IIR filter was simulated in Modelsim and the following waveforms were obtained. (Figure 4)After checking the filtered output the delay between the input signal and the output signal was calculated from the Modelsim wave window (Figure 4)

The input wave consisting of the two waves has been shown in fig below.
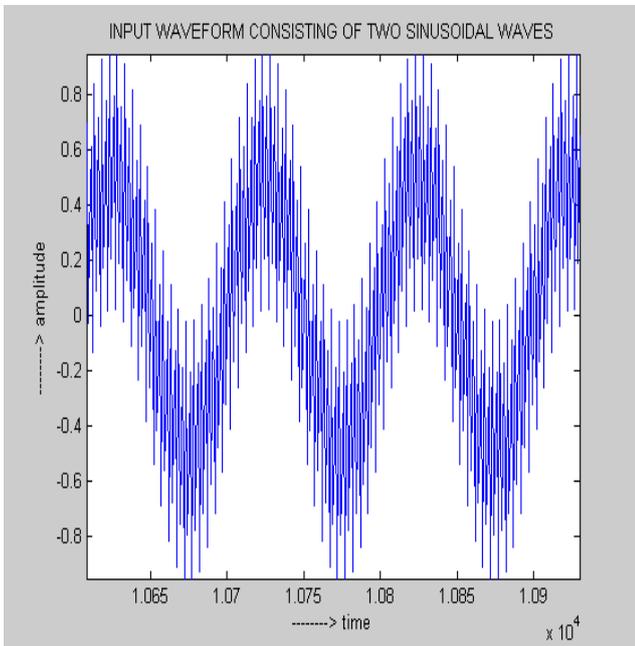

Figure5:input wave consisting of two sine waves

When input wave has been applied to digital filter the output consists of one wave form which is desired wave and all other waves has been removed by the filter.As shown below out of two input waves only required wave is obtained in output.Basically all other waves are Noises which are added in ECG signal .
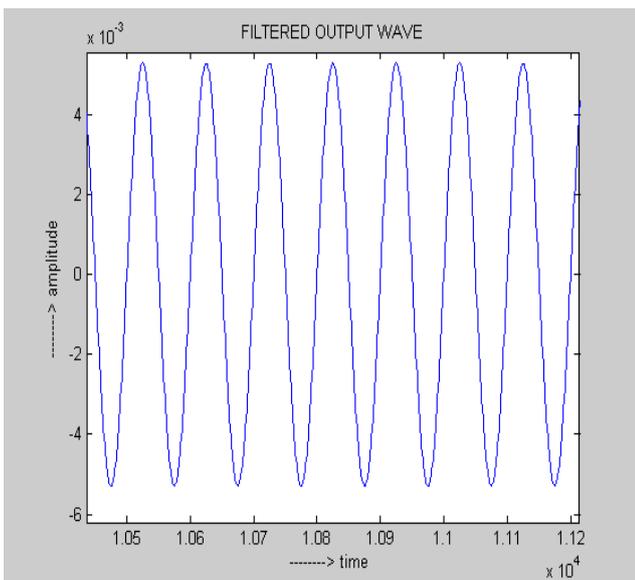
Figure 6: Output of the filter when the input of figure 5 was given as input

After that numerator and denominator coefficients has been calculated which has been shown in following Figures
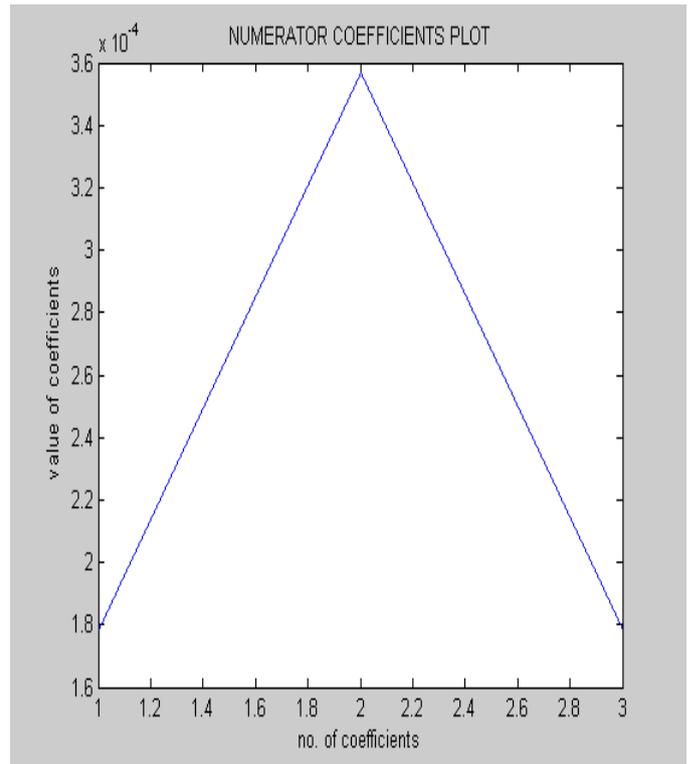
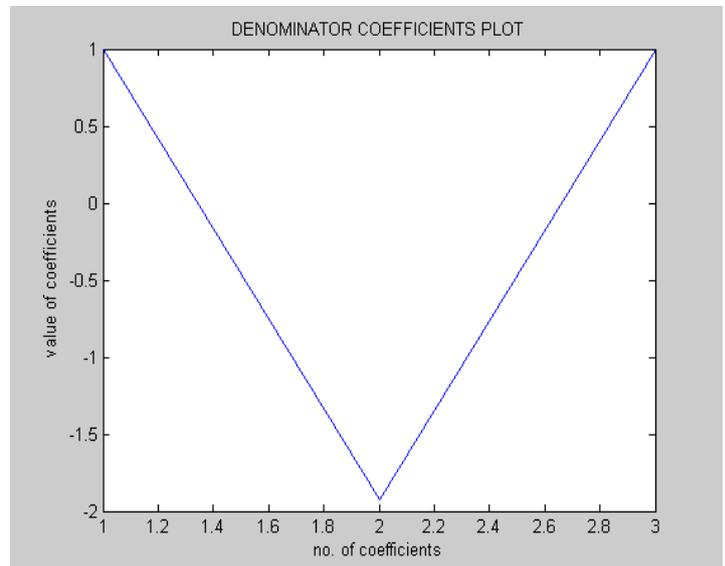Figure 7: Plot of numerator coefficients of IIR filter designed

Figure 8: Plot of denominator coefficients of IIR filter designed

Finally FPGA kit has been burned and slots has been finalised or reserved for various components used in IIR filter. A burned FPGA kit has been shown in figure.
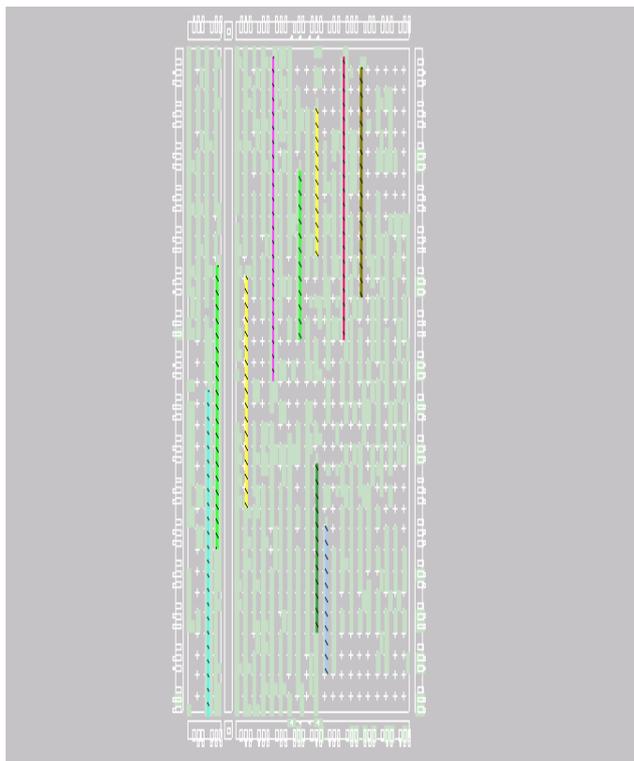
Figure 9: FPGA kit

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