Next Generation Micro-power Systems

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Abstract— Emerging micro-systems such as portable and implantable medical electronics, wireless micro-sensors and next-generation portable multimedia devices demand a dramatic reduction in energy consumption. The ultimate goal is to power these devices using energy harvesting techniques such as vibration-to-electric conversion or through wireless power transmission. A major opportunity to reduce the energy consumption of digital circuits is to scale supply voltages to 0.5V and below. The challenges associated with ultra-low-voltage design will be presented. These include variation-aware design for logic and SRAM circuits, efficient DC-DC converters for ultra-low-voltage structuring to support extreme parallelism. This paper also addresses micro-power analog and RF circuits, which require the use of application specific structures and highly digital variation-aware architectures.

Index Terms— Micro-System, SRAM, RF Circuit

I. INTRODUCTION

In the near future, a number of systems will be powered using energy scavenging technologies, enabling exciting new applications such as medical monitoring, toxic gas sensors and next-generation portable video gadgets. This will require the electronic circuits to operate with utmost energy efficiency while performing the required functionality. Energy minimization requires a system-level approach optimizing not only the signal processing and interface circuits but also the energy processing function. The energy per operation of digital logic continues to improve with process scaling. However, energy savings are limited by device impairments such as random dopant fluctuations. Operating circuits at or below 0.5V requires a departure from traditional circuit approaches (e.g., the use of redundancy). In the mixed-signal micro-power domain, the designer should develop structures that mitigate or even exploit device variability Application specific architectures apply not only to digital but also mixed-signal circuits for energy minimization. Similarly, energy processing circuits must be carefully optimized for both the load circuits and the energy source. This requires run-time optimization rather than static design-time optimization. Circuits should be biased at their minimum energy point accounting for variations in signal statistics and environmental conditions. A systems-level approach to the energy problem can result in more than an order of magnitude energy reduction compared to present day systems.

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II. ENERGY SOURCES AND DELIVERY

A. Energy Scavenging Technology

The ability to harvest ambient energy through energy scavenging technologies is necessary for battery-less operation. A 1cm3 primary lithium battery has a typical energy storage capacity of 2800J [7]. This can potentially supply an average electrical load of 100µW for close to a year but is insufficient for systems where battery replacement is not an easy option (e.g., implantable medical electronics and embedded wireless micro-sensors).

[Table I: Examples of energy harvesting sources]

Source	Source	Output Power	Comments
Photovoltaic	Gullar [1]	5µW	150µm x 150µm, 20k LUX
	Das [2]	120µA/cm²	Protein based, 10W/cm² excitation
Thermal	Lhermet [3]	4µW/cm²/°c	1V at ΔT = 60°c
	Leonov [4]	250µW	Ambient indoor temperature
	Stark [5]	24µW	2.7V at ΔT = 5°c
Vibrational	Renaud [6]	40µW	Piezoelectric, 35mg mass, 1.8kHz
	Roundy [7]	335µW	Piezoelectric, 2.25ms⁻², 60Hz

Table I shows the output power levels generated by energy harvesting techniques [1-7]. The most common harvesters transduce solar, vibrational or thermal energy into electrical energy. The vibrational harvesters use one of three methods: electromagnetic (inductive), electrostatic (capacitive) or piezoelectric. The thermoelectric harvesters exploit temperature gradients to generate power. Most harvesters in practically usable forms can provide an output power of 10 – 100µW (Table I), setting a constraint on the average power that can be consumed by the load circuitry for self-powered operation. It is also possible to extract energy from electromagnetic radiation emitted by RF sources (this generates tens of µW's and has been used in RFID tags and several implanted medical devices).

B. Energy Processing Circuits

Extracting the maximum energy from a battery or from energy harvesting sources requires optimized energy processing circuitry.

The energy processor must not only provide the desired voltage and current to the load circuitry, but should also account for the source characteristics, load variations (e.g., signal activity), and environmental variations to optimize overall system energy. For energy harvesting sources, energy processing begins with circuitry to rectify/condition the voltage or current obtained from the energy harvester and to store the energy in an intermediate storage medium before being fed to a voltage regulator. Secondary batteries and super capacitors can be used as an *energy buffer* during periods of low harvester output or when the load requires a large instantaneous power. A key challenge in micro-power systems is that the delivered load power can be sub-10µW, driving the need for highly efficient energy processing control structures. A buck converter design (with external passives) optimized with all-digital control circuitry can achieve >80% efficiency down to 1µW load power levels [8]. At these light loads, pulse-frequency modulation (PFM) is an effective technique to achieve high efficiency. However, minimizing the number of external components is highly desirable in embedded medical applications. Switched capacitor designs are attractive in this regard as the power conversion circuitry can be completely integrated on-chip. A switched capacitor converter that uses multiple gain settings, charge recycling techniques and PFM control to provide *variable* supply voltages achieves >70% efficiency from 3µW up to 500µW load power [9].

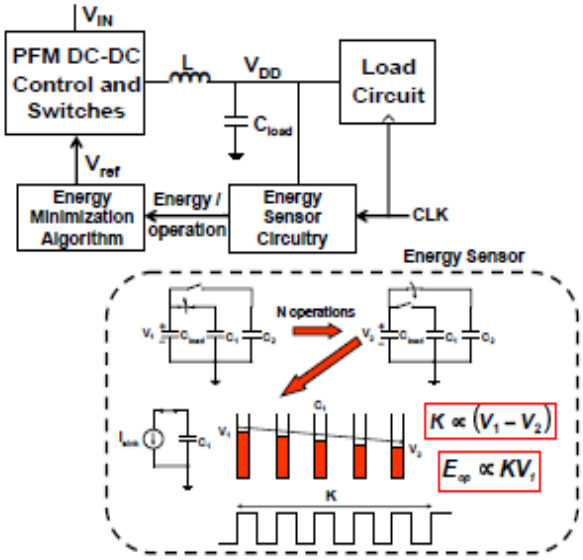

Fig. 1 Block diagram of a minimum energy tracking loop with an embedded DC-DC converter.

Operating digital circuits at their minimum energy operating voltage (MEP) [8] is important in energy critical applications. The minimum energy of a digital circuit is obtained by balancing the switching and leakage energy as the supply voltage is varied. The minimum energy tracking loop shown in Fig. 1 works alongside the DC-DC converter to automatically track the MEP of arbitrary digital load circuits with changing workload and operating conditions. The energy sensor circuitry provides a normalized representation of the energy consumed per operation (Eop), which is then used by a slope-tracking algorithm to arrive at the MEP. The ability to change the MEP with varying operating conditions helps reduce the energy consumption of the load circuit by 50%. The tracking methodology is independent of the size and type of the digital load circuit and the topology of the DC-DC converter being used. A higher leakage to active energy ratio (e.g. due to scaling from 65nm to 22nm) pushes the MEP to a higher voltage.

III. ULTRA-LOW-VOLTAGE DIGITAL SIGNAL PROCESSING

Voltage scaling continues to be the dominant strategy for energy minimization in digital logic and memory circuits. In applications with relaxed switching speed constraints, digital circuits can be operated at the MEP, which typically lies in the sub-threshold region (VDD < VT). In systems with higher throughput constraints, such as video decoding or baseband communications, VDD can still be substantially lowered (e.g. to 0.5V) while using parallel architectures to mitigate the speed loss [10]. For memory circuits that must be powered for an arbitrarily long time, voltage scaling significantly reduces leakage power.

However, ultra-low-voltage design must overcome the key challenge of process variation, whose effects worsen at decreased voltages. Nevertheless, robust ultra-low-voltage operation is achievable with the appropriate design methodologies, circuit assists, and architectures.

A. Variation-Aware Logic Design

At low voltages, process variation and reduced ION/IOFF ratios adversely affect operation of logic circuits. Output levels can be degraded such that even static CMOS logic no longer provides guaranteed functionality. One way to mitigate local variation is to upsize devices in logic gates, using a statistical approach to optimally size for functionality while minimizing energy overhead. Circuit delay uncertainty also increases drastically at ultra-low-voltages, as shown by Monte Carlo simulations of 30k timing paths in a 0.3V, 65nm microcontroller (Fig. 2). Statistical timing approaches such as those described in [9] and [11] are essential for future micro-power systems. Variation-tolerant architectures will play an important role by allowing detection and correction of transient errors during run-time [12].

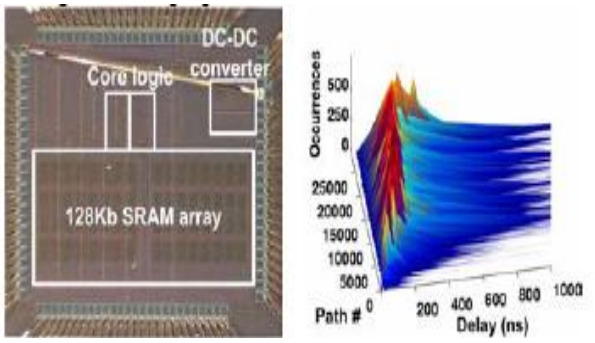

Fig. 2 Die photo of sub-Vt microcontroller [9] and Monte Carlo simulation of its 30k timing paths at 0.3V.

B. SRAM

The 6T bit-cell depends on ratioed sizes to achieve adequate read and write margins. However, the ratioed fight between access and driver devices reduces cell stability during a read. At low voltages, variation can easily overwhelm the small read margin set by sizing, causing read failures. The SRAM in [13] demonstrates one approach to enable sub-VT operation.

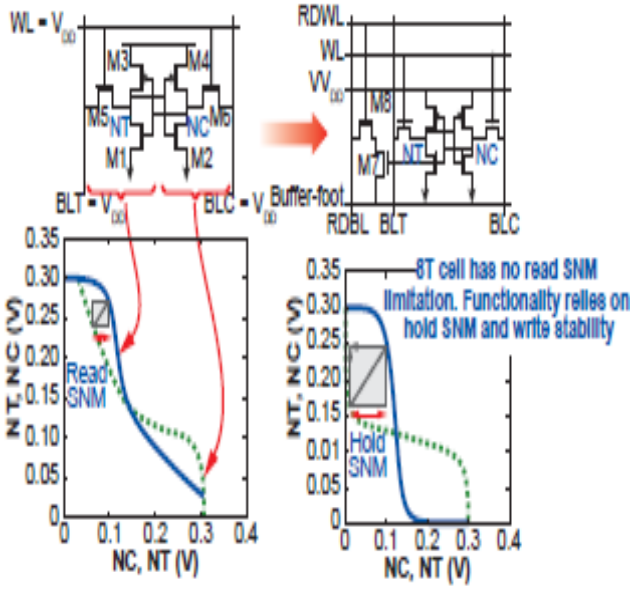

Fig. 3 Read SNM limitation is removed in the 8T bit-cell [13].

The 8T cell (Fig. 3) removes the read margin limitation by isolating the storage node from the read bit line. Crucial circuit assists enforce the relative device strengths required for functionality. For example, during a write, the cell supply voltage is reduced, weakening the PMOS devices relative to access devices. During a read, the feet of all un accessed read buffers are pulled to VDD, eliminating their sub-VT leakage currents which would otherwise degrade the read bit line voltage.

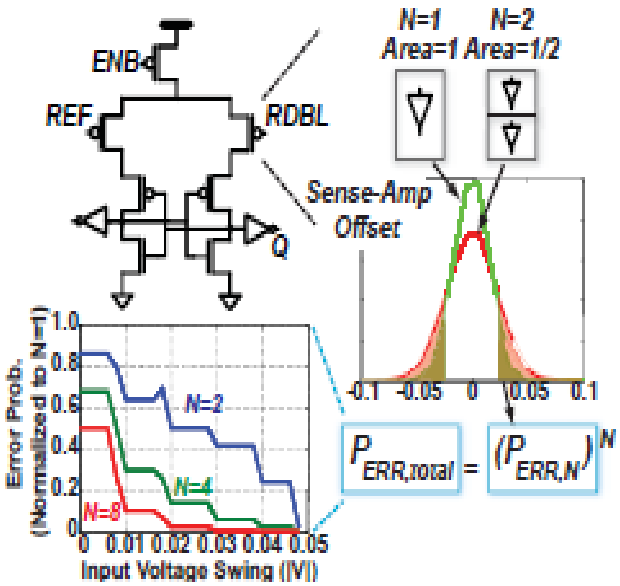

Fig. 4 Redundancy significantly reduces the error probability in the SRAM sensing network [13].

Redundancy is a powerful technique for managing variation in ultra-low-voltage systems. In sense amplifiers, redundancy eases the trade-off between physical area and probability of error in sensing due to offset variation. Instead of a single full size sense-amplifier, N smaller copies can be created within the same area. Due to their smaller devices, these redundant copies exhibit wider offset distributions. However, the overall error probability is now the probability that *all* N sense-amplifiers fail. As shown in Fig. 4, even a small amount of redundancy (N=2) significantly reduces the error probability. A 0.3V system on- a-chip in 65nm (Fig. 2) demonstrates the above techniques in a 16b microcontroller and an 8T SRAM [9]. The low voltage and power level is supplied by an efficient, fully integrated DC-DC converter.

IV. ENERGY EFFICIENT ANALOG PROCESSING AND CONVERSION

Micro-power systems typically require ADCs with low to-moderate resolution and rate. As thermal noise is not a challenging design constraint, the ADC supply voltage can be reduced to enable low energy operation. Energy efficiency requires variation-tolerance, parallelism, application specific architectures, and digital structures.

A. Variation-Tolerant Architectures:

Mismatch and variation ultimately limit performance and yield of ADCs. Offset compensation techniques can be applied to mitigate these limitations and enable low power operation. For example, offset compensated regenerative amplifiers allow for reduced gain in non-regenerative pre-amplifiers thereby reducing power. In a micro-power SAR ADC [14], a regenerative amplifier has been demonstrated that dramatically reduces input offsets through an analog feedback loop. SAR is an excellent topology for micro-power applications, as demonstrated by a 10b ADC in 65nm requiring 4.4 fJ/conversion step [15]. Extreme variation can be compensated with redundancy and digital feedback. In [16], a 6b flash ADC leverages comparator redundancy to tolerate comparator offsets many times larger than an LSB step size while enabling sub-threshold operation at supply voltages down to 200mV. The ADC uses digital common-mode feedback to reduce the effects of common-mode input offsets. *Parallelism:* An approach to achieve energy efficient high rate operation is to bias many time-interleaved ADC converters in the sub-threshold regime using extreme parallelism. For these highly parallel systems, variation and clock skew can limit performance and redundancy is a powerful tool that can be exploited to improve yield. For example, in [17], a 36-channel time-interleaved SAR ADC employs 6 additional redundant channels that can replace poorly performing channels.

B. *Application Specific Architectures*

To minimize energy, it is imperative to analyze the ADC in conjunction with the other elements. Fig. 5 presents a carbon-nanotube (CNT) chemical sensing system that leverages the device attributes to minimize energy consumption [18].

The impedance of CNTs varies due to toxic chemicals, and to measure this change in the presence of extreme CNT variation requires a DAC and ADC with a cumulative resolution of 18b. With accurate energy models of both blocks, a 10-to-12b ADC and 8-to-6b DAC were found to minimize overall energy.

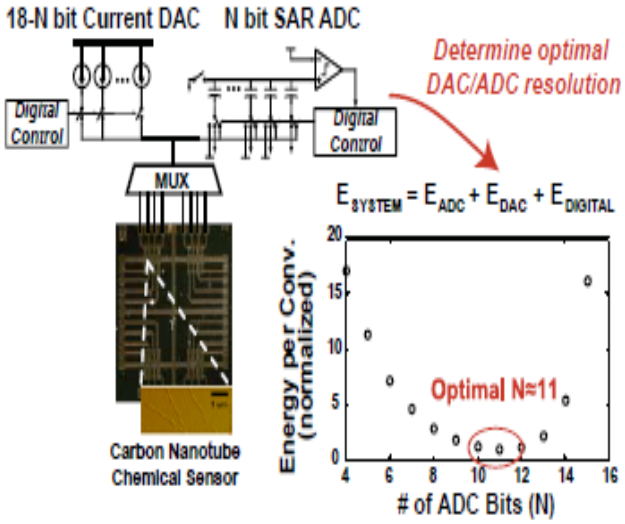

Fig. 5 Block diagram of a carbon nanotube chemical sensing system [18].

C. *Comparator Based Analog Circuits*:

Comparator-based structures allow the implementation of switched capacitor ADCs and analog circuits without the need for analog feedback – comparators replace the functionality of OpAmps by controlling charge transfer through comparator switching events rather than forcing a virtual ground through feedback. This approach offers potential for reduced power consumption and to address scaling issues in emerging technologies [19].

V. LOW-RATE RADIO ARCHITECTURES AND CIRCUITS

Wireless communication links found in micro-power systems dominate the overall device energy consumption. This is true despite the relatively low average data rates (tens of kbps) and short (<10m) distances required by these devices. A number of wireless standards address this space including Bluetooth, MICS, and Zigbee (802.15.4 and 802.15.4a). Two emerging trends in micro-power radios are to leverage highly digital architectures and to exploit high quality passive components such as Bulk Acoustic Wave (BAW) resonators. To reduce energy requirements, it is advantageous to use a radio that can rapidly turn-on and can transmit data at a fast instantaneous data rate. Highly digital RF circuits are well suited to these demands, as they consume no static bias currents and can be quickly enabled and disabled. Moreover, they allow for highly integrated, reconfigurable, low-cost radios [20]. An example of a highly digital, ultra-wideband (UWB) transceiver that achieves micro-power operation is shown in Fig. 6 [21][22]. It communicates via 2ns, non-coherent UWB pulses in one of three 500 MHz channels in the 3-5 GHz band. The transmitter is digital and dissipates only CV2 power. Pulses are generated by combining multiple edges from a calibrated digital delay line and the power amplifier is implemented using inverters. The receiver uses non-coherent, integrating energy detection architecture. Both transmitter and receiver can turn-on within 2ns. The transmitter requires 47pJ/pulse, where one pulse is transmitted per bit, and the receiver requires from 0.85-to-2.5nJ/bit.

For extremely power constrained applications, external high quality factor components such as BAW resonators or filters can be used by a receiver to precisely filter out interferers or generate an ultra-low power, highly stable oscillator. For example, in [23], a BAW filter performs channel selection, allowing for an imprecise but low power un tuned digital ring oscillator to drive a mixer.

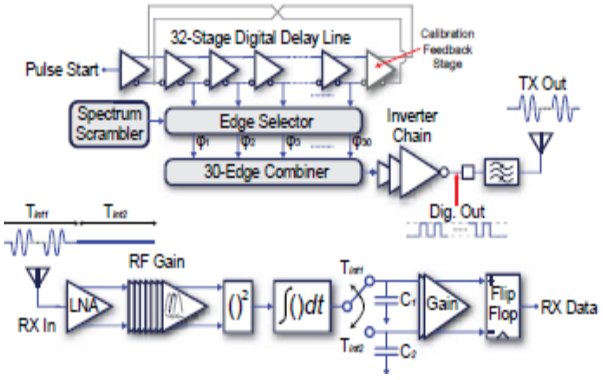

Fig. 6 Block diagram of an ultra-wideband transceiver chipset that utilizes highly digital and low-voltage architectures.

VI. CONCLUSIONS

To operate future micro systems through energy scavenging, the power dissipation of electronics must be dramatically reduced. The design of micro-power electronics requires a system-level design approach involving variation-tolerant architectures, ultra-low voltage circuits, and highly digital RF circuits. Such self powered electronics will be a key enabler of exciting new applications such as implantable medical devices.

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