

# A Comprehensive Study on Failure Modes and Mechanisms of Thin Film Chip Resistors

Sarat Kumar Dash, Sandhya V. Kamat



Abstract: Usually, resistors and capacitors populate majority portion of a common electrical circuit, hence miniaturization drive of any package or subsystem starts with miniaturized resistor and capacitors. In this context, thin film chip resistors are the most sought-after components for any electronic/electrical circuit due to their small size, wide range of values, military temperature range, stringent tolerance, low TCR value (recognised with PPM). Increased use of thin-film surface mount chip resistors in military and space application has led to an increased awareness of its potential failure modes in harsh environments. Thin film resistor with lower TCR (5PPM, 10PPM and 25PPM) are most preferable and widely used because of very low temperature coefficient of resistance (TCR) and high resistivity, which suits for high precision measurement application. Low temperature coefficients characteristics of thin film resistors also makes them stable and reliable. Because of their high-volume usage in recent times, failure in thin film resistor with lower TCR/PPM (Parts per Million) are also being seen more predominantly. In general, there are two types of thin film chip resistors, one is discrete type and the other is die type or wire bondable type. Discrete type chip resistor are used directly on cards, whereas, die type/wire bondable type chip resistors used in hermetically sealed HMC packages. Standard failure mode of a resistor is open mode or high resistance mode, whereas short mode failure has a very low probability. Hence in this paper, failure modes and mechanisms of both types of thin film chip resistors, with respect to common failure causes such as EOS, ESD are discussed, which is in continuation to Fabrication/Workmanship related failures discussed in our earlier technical paper. With this, all possible failure modes and mechanism related thin film chip resistors are explained. Discussion in totality always provide in depth analysis on a subject of concern, which in turn facilitate reliability assessment of the component and corrective action, if any.

Key Words: Electrical Overstress (EOS); Electrostatic Discharge (ESD); Temperature Co-efficient of Resistance (TCR); Parts Per Million (PPM); Moisture Ingression; Corrosion, Hybrid Micro Circuit (HMC)

#### I. INTRODUCTION

Chip resistors are a type of resistor among passive components and are mainly used to lower the circuit voltage and limit the current in electronic products. They are essential components of the majority of high-tech electronic products.

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Chip resistors have many advantages such as small size, light weight and no inductance, and they are widely used in electronic equipment and populated PCBs for adapting to high density surface mount. The chip resistors can be divided into thin-film chip resistors and thick-film chip resistors. The former offers better precision and lower temperature coefficients, which means more stable and reliable resistance. With the development of high precision electronic devices, thick film chip resistors are unable to meet higher performance requirements because of high temperature coefficient of resistance. Therefore, thin film chip resistors are most preferable because they have low temperature coefficients, which makes them stable and reliable. The predominant films systems used in the manufacture of thinfilm resistors today are nickel-chrome and tantalum nitride [1]. The vast majority of these, however, are derivatives of Nickel-Chrome (Ni-Cr) or Tantalum Nitride (TaN). Ni-Cr thin film has a low temperature coefficient of resistance (TCR) and high resistivity, which increase its importance and technical applications as a resistor in the electronic industry field [2-4][7][8]. However, in the case of thin film chip resistors or other miniature products, it is necessary to encapsulate the film and prevent corrosion in humid environments [5][9]. Increased use of thin-film surface mount chip resistors in military and space application has led to an increased awareness of potential failure modes in harsh environments.

In order to understand the failure mode and mechanism of thin film chip resistor, it is necessary to know about their physical construction. Construction of thin film resistor (discrete type) was already explained in earlier publication [6], however, for the sake of completeness construction of both types of film resistors (discrete type and wire bondable/die type) are shown in figure-1 and figure-2 respectively. Usually, thin film resistors are fabricated by vacuum evaporation or sputtering of thin films of resistive materials (mostly Nichrome) directly on top of the ceramic substrate or silicon wafer. These materials exhibit good adhesion on the oxide as thin films, and are usually built with a film thickness of about 100-1000Å. The value of a thin film resistor can be set precisely to its final value by laser trimming. For discrete type thin film resistor, both side of the chip there are solder coated nickel end-cap for electrical contact of the chip resistor. The resistor film (Nichrome) is protected by a passivation layer of thickness ≤10µm and covered by hard epoxy coating. The role of passivation layer is very critical in chip resistor as it protect the resistor film from moisture and contaminants. By virtue of their construction, passivation layers and end cap are very sensitive for temperature excursion, which the chip resistor usually encounter during manual soldering or post-reflow solder touch-up.

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Improper fabrication process of thin film chip resistors usually ends up in moisture induced open mode failure as a result of corrosion of internal resistive material [6].

For wire bondable/die type thin film resistor, aluminium bond pads are provided along with resistive thin film track for wire bond connection. Thin film materials are same as that of discrete type thin film chip resistor (Nichrome), but there is no passivation layer in case of wire bondable/die type thin film resistor. Therefore, these types of resistors are supposed to be used inside hermetically sealed packages.

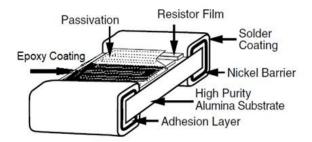


Figure-1: Internal Construction of Discrete Thin Film Chip Resistor

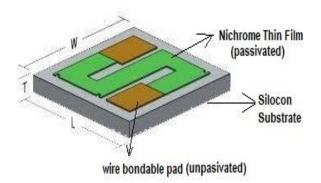


Figure-2: Internal Construction of Wire-Bondable (Die Type) Thin Film Chip Resistor

Electrical Overstress (EOS), Electrostatic Discharge (ESD) and Fabrication/Workmanship Induced failures are the major failure causes of EEE components, which were source screened and qualified as per respective MIL/ESA/NASA standards. Manufacturing related defect or component design related defect, if any, usually wedded out as a part of screening. Thin film chip resistors, used in onboard application of ISRO projects, being source screened and high reliability part, hence it is prudent to understand various failure modes and mechanism, which in turn helps in finding out the root cause of failure and subsequent corrective actions.

# II. REFERENCE TO EARLIER SIMULATION STUDY ON THIN FILM CHIP RESISTORS

In an earlier study, fabrication/workmanship induced failure simulation experiments were carried out on discrete type thin film chip resistors RM1206, 0.1%, 25PPM, 1/8W (many values) in order to understand the root cause of failure of large number of thin film resistors in may satellite project during various ground level tests [6]. Simulation study was conducted on Nichrome based thin film resistors, as these types of chip resistors are used in ISRO projects and following conclusions were made.

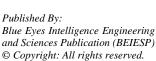
- > Thin film resistors soldered using proper soldering method (either manual/re-flow) did not showed any time dependent failure even with biased with higher voltage. However, open mode failure of one  $100k\Omega$  resistor, which was reflow soldered, showed the reliability concern in Nichrome based thin film resistor. In this case, there can be two possibilities for open mode failures, i.e., either there is multiple solder touch-up for this particular resistor after reflow soldering for what so ever reason or the passivation layer for this particular piece has a manufacturing defect. The first reason is slightly unlikely as reflow soldering process was carried out on the resistors under strict Quality Control (QC) guidance. There is a possibility for the second reason as thin film resistor do not have any screening test that could weed out defects such as crack and porosity in the passivation layer. Therefore, Nichrome based thin film resistor are not environment friendly.
- In order to establish the exact failure mechanism for open mode failure in Nichrome based thin film resistor, biased humidity test was conducted on the chip resistor. As per the test results, when the solder time is more than 15sec, those resistors, even though do not show any anomalies immediately after soldering, subsequently failed in open mode after different time of testing. There are two interesting facts observed from that simulation study; (i) as the soldering time increases, time for open mode failure in the resistors decreases, (ii) the time taken for higher value resistor is lesser than those of lower value resistors. From above two observations, failure mechanisms for open mode failure in chip resistor can be explained as follow. As the soldering time increases, damage probability to the passivation layer increases so also the probability of moisture ingression, which resulted in oxide formation of the Nichrome metal and finally the metal film failed in open mode. Hence, the failure mechanism in this case can be related to corrosion.
- From the above discussion, it is inferred that open mode failure in Nichrome based thin film chip resistor is time dependant and related to moisture induced corrosion.

# III.FURTHER SIMULATION STUDIES ON THIN FILM CHIP RESISTORS

In order to understand few other failure mechanisms in both discrete type thin film chip resistors and wire bondable/die type thin film resistors few more simulation studies were conducted and they are as follows

- (a) Electrical Overstress (EOS) Simulation Study on discrete type thin film chip resistors RM1206, 0.1%, 25PPM, 1/8W (few values).
- (b) Electrostatic Discharge (ESD) Simulation Study on discrete type thin film chip resistors RM1206, 0.1%, 25PPM, 1/8W (few values).
- (c) Electrostatic Discharge (ESD) simulation study on die/wire bondable type thin film chip resistors RM1206, 0.1%, 25PPM, 1/8W (few values).

The details of the studies are explained in the subsequent subsections.







## **Electrical Overstress (EOS) Simulation Study on** Discrete Type Thin Film Chip Resistors RM1206, 0.1%, 25PPM, 1/8W (Few Values)

Electrical Overstress (EOS) is one of the very common failure cause in EEE components, happened due to improper testing/test procedures or handling. In order to find out the susceptibility of discrete thin film chip resistors towards electrical overstress few chip resistors RM1206, 0.1%, 25PPM, 1/8W (different values) were subjected to EOS through step stress method. Following steps were adopted in the course of aforesaid simulation study.

a. Initial Visual Examination and Electrical Measurement of Chosen Components:

RM1206, 0.1%, 25PPM, 1/8W (five values, 2nos. each) were chosen for the study. Details about the components are shown in table-1.

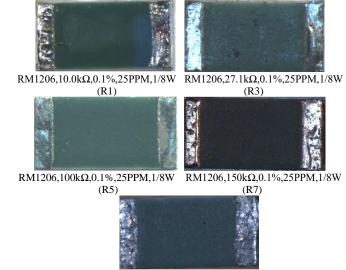
**TABLE-1: Components Details Taken for Simulation** Study

Resistor Type	Resistance Value	Sample Nos.	Sample Marking
RM1206EB,	$10.0$ k $\Omega$	2nos.	R1 to R2
±0.1%, 25PPM,	$27.10$ k $\Omega$	2nos.	R3 to R4
1/8W	$100.00$ k $\Omega$	2nos.	R5 to R6
	150.00kΩ	2nos.	R7 to R8
	301.00kΩ	2nos.	R9 to R10

Chip resistors were visually inspected using optical microscope at 100X. No visual anomalies were observed. Optical photographs of few chip resistors are shown in figure-3. Values of the chip resistors were chosen based on the feedback from field failure data. Initial electrical test results of each resistor are shown in table-2.

**TABLE-2: Initial Electrical Measurement Result of Chip Resistors** 

Sample	Measured	Specified	Sample	Measured	Specified
No.	value in kΩ	Limit in kΩ	No.	value in kΩ	Limit in kΩ
R1	9.992	9.90 to	R7	150.075	149.85 to
R2	10.009	10.01	R8	150.098	150.15
R3	27.102	27.073 to	R9	300.947	300.699 to
R4	27.098	27.127	R10	301.078	301.301
R5	99.927	99.9 to			
R6	99.981	100.1			



RM1206,301kΩ,0.1%,25PPM,1/8W (R9)

Figure-3: Optical Image of One Resistor from Each Value Shows no Visual Anomalies

b. EOS simulation study by Step Stress Method:

As per the data sheet voltage rating of thin film chip resistors RM1206, 0.1%, 25PPM, 1/8W is 100V. EOS simulation study was conducted on the chip resistors by applying voltage started from 100V up to 220V (>double the rating) in a step of 20V initially and then in a step of 10V after 180V. For lower values resistors, power dissipation limit, exceeded the specified limit from beginning of test, whereas for higher value resistors power dissipation limit exceeded with application of higher voltages. A Lambda make power supply (300V, 5A) was used for voltage application and a sixdigit multi-meter (make: Keysight, model: 34401A) was used for current measurement. The resistors were mounted on a card using reflow soldering and the terminations were connected with 26AWG wires (~5cm length) as a provision for voltage application. The results are shown in Table-3.

**TABLE-3: EOS Simulation Test Result** 

<b>Initial Values</b>	Applied Voltage in Volt (v), Voltage Applied for ~30sec and Gap					pplied fo	or ~30s	Remarks		
of Resistors in			between Voltage Application ~2 min				min			
$\mathbf{k}\mathbf{\Omega}$	100	120	140	160	180	190	200	210	220	
		Me	easure Cu	irrent Ac	ross Each	n Resisto	r in m/	A		
9.992 (R1)	10.09	12.008	14.010	16.011	18.014	19.013	6.608			At application of 200V, resistance value changed to 28.750kΩ
										and current decreases appropriately.
10.009(R2)	9.911	11.891	13.874	15.856	17.838	18.830	4.197			At application of 200V, resistance value changed to 45.270kΩ
										and current decreases appropriately.
27.102(R3)	3.688	4.427	5.165	5.902	6.641	7.010	7.37	4.830		At application of 210V, resistance value changed to $41.4k\Omega$ and
										current decreases appropriately.
27.098(R4)	3.69	4.428	5.166	5.904	6.642	7.011	7.38	5.025		At application of 210V, resistance value changed to $39.8k\Omega$ and
										current decreases appropriately.
99.927(R5)	1.00	1.2	1.4	1.6	1.8	1.9	2.0	2.1	1.349	At application of 220V, resistance value changed to 155.6k $\Omega$ and
										current decreases appropriately.
99.981(R6)	1.00	1.2	1.4	1.6	1.8	1.9	2.0	2.1	2.2	The resistor did not degrade even after application of 220V.
150.075(R7)	0.666	0.799	0.932	1.066	1.199	1.266	1.332	1.399	1.465	The resistors did not degrade even after application of 220V.
150.098(R8)	0.666	0.799	0.932	1.066	1.199	1.266	1.332	1.399	1.465	
300.947(R9)	0.332	0.398	0.465	0.531	0.598	0.631	0.664	0.697	0.731	The resistors did not degrade even after application of 220V.
301.078(R10)	0.332	0.398	0.464	0.531	0.597	0.631	0.664	0.697	0.730	

NOTE: Resistor R3 and R4 were de-capped after simulation study and optical photograph revealed internal resistive patterns are melted and partially discontinued at certain location due to electrical overstress (refer figures-4 &5). However, this signature is not similar to and Advanced Technology

induced corrosion related failure.

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Figure-4: Localized Melting of Resistive Tracks of the Degraded Resistor R3

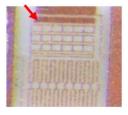


Figure-5: Localized Melting of Resistive Tracks of The Degraded Resistor R4

# B. ESD Simulation Study on Discrete type Thin Film Chip Resistors RM1206, 0.1%, 25PPM, 1/8W (Few Values)

Electrostatic Discharge (ESD) is one of the very common failure causes in EEE components, happened due to improper testing/test procedures or handling. In order to find out the susceptibility of discrete thin film chip resistors towards electrostatic discharge, few chip resistors RM1206, 0.1%, 25PPM, 1/8W (different values) were subjected to ESD through step stress method. Following steps were adopted in the course of aforesaid simulation study.

a. Initial Visual Examination and Electrical Measurement of Chosen Components:

RM1206, 0.1%, 25PPM, 1/8W (four values, 5nos. each) were chosen for the study. Details about the components are shown in table-4.

TABLE-4: Components Details Taken for Simulation Study

Resistor Type	Resistance Value	Sample Nos.	Sample Marking
RM1206EB,	10.0kΩ	5nos.	R1 to R5
±0.1%,	$20.0$ k $\Omega$	5nos.	R6 to R10
25PPM,	33.2kΩ	5nos.	R11 to R15
1/8W	301.00kΩ	5nos.	R16 to R20

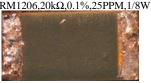
Chip resistors were visually inspected using optical microscope at 100X. No visual anomalies were observed. Optical photographs of few chip resistors are shown in figure-6. Values of the chip resistors were chosen based on the feedback from field failure data. Initial electrical test results of each resistor are shown in table-5.





RM1206,10kΩ,0.1%,25PPM,1/8W RM1206,20kΩ,0.1%,25PPM,1/8W





 $RM1206, 0.1\%, 33.2 k\Omega, 25 PPM, 1/8W\ RM1206, 0.1\%, 301 k\Omega, 25 PPM, 1/8W$ 

Figure-6: Optical Image of One Resistor from Each Value Shows no Visual Anomalies

TABLE-5: Initial Electrical Measurement Result of Chip Resistors

Sample No.		Specified Limit in kΩ		value in	Specified Limit in kΩ
R1	9.994	9.90 to	R11	33.178	33.166 to
R2	10.009	10.01	R12	33.182	33.233
R3	10.008		R13	33.201	
R4	9.996		R14	33.198	

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R5	10.005		R15	33.216	
R6	20.012	19.98 to	R16	300.947	300.699 to
R7	20.009	20.02	R17	301.078	301.301
R8	20.010		R18	301.291	
R9	19.989		R19	301.105	
R10	19.995		R20	300.867	

b. ESD simulation Study by Step Stress Method:

To understand the effect of ESD on thin film chip resistors above resistors were subjected for ESD simulation study. Resistors above  $10k\Omega$  were chosen based on the feedback from reported failure. Almost 95% of chip resistor failed in open mode are having value  $\geq 10k\Omega$ . All the above resistors were hand soldered and mounted on the card with proper precautions. Wire termination (~5cm) was provided with each resistor for proper application of ESD stress. ESD pulses were applied with Human Body Model ESD simulator as per MIL-STD-883K method 3015.7. ESD pulses were applied by step stress method in a step of  $\pm 1000$ V starting from  $\pm 1000$ V. However, a final applied ESD pulse is shown for the sake of brevity. Pre and post-ESD resistance measurement was carried out on the chip resistors and the obtained test results are shown in table-6.

Table-6: ESD Simulation Test Results on RM1206 Chip
Resistors

2	†	SISt.	OIB		
	Resistor Type	Sl.	Measured	Applied	Measured
		No.	Resistanc	ESD	Resistanc
			e (Initial)	Pulses	e
				(5 pulses)	(Final)
	RM1206 10.0kΩ 0.1% 1/8W-R	R1	$9.998 \text{ k}\Omega$	±6000V	$9.998 \text{ k}\Omega$
	RM1206 10.0kΩ 0.1% 1/8W-R	R2	$9.997~k\Omega$	±6000V	$9.997~k\Omega$
	RM1206 10.0kΩ 0.1% 1/8W-R	R3	$10.003 \text{ k}\Omega$	±6000V	$10.003 \text{ k}\Omega$
	RM1206 10.0kΩ 0.1% 1/8W-R	R4	$10.002~k\Omega$	±6000V	$28.5 \text{ k}\Omega$
	RM1206 10.0kΩ 0.1% 1/8W-R	R5	$9.996~\mathrm{k}\Omega$	±6000V	$9.996~\mathrm{k}\Omega$
	RM0505 20.0kΩ 0.1% 1/40W-S	R6	$20.002 \text{ k}\Omega$	±7000V	$20.002 \text{ k}\Omega$
	RM0505 20.0kΩ 0.1% 1/40W-S	R7	$20.005 \text{ k}\Omega$	±7000V	$48.7 \text{ k}\Omega$
	RM0505 20.0kΩ 0.1% 1/40W-S	R8	$19.996 \mathrm{k}\Omega$	±7000V	$19.996 \text{ k}\Omega$
	RM0505 20.0kΩ 0.1% 1/40W-S	R9	$19.997 \text{ k}\Omega$	±7000V	$19.997 \text{ k}\Omega$
	RM0505 20.0kΩ 0.1% 1/40W-S	R10	$20.005 \text{ k}\Omega$	±7000V	$20.005 \text{ k}\Omega$
	RM1206 33.2kΩ 0.1% 1/8W-R	R11	$33.202 \text{ k}\Omega$	$\pm 8000V$	$33.202 \text{ k}\Omega$
	RM1206 33.2kΩ 0.1% 1/8W-R	R12	$33.198k\Omega$	$\pm 8000 V$	$33.198k\Omega$
	RM1206 33.2kΩ 0.1% 1/8W-R	R13	$33.197 \text{ k}\Omega$	±8000V	$33.197 \text{ k}\Omega$
	RM1206 33.2kΩ 0.1% 1/8W-R	R14	33.203 kΩ	±8000V	$33.203 \text{ k}\Omega$
	$RM1206\ 33.2k\Omega\ 0.1\%\ 1/8W-R$	R15	$33.202 \text{ k}\Omega$	$\pm 8000V$	$33.202 \text{ k}\Omega$
	RM1206 301.0kΩ 0.1% 1/8W-S	R16	$301.03 k \Omega$	$\pm 8000V$	$301.03 k \Omega$
	RM1206 301.0kΩ 0.1% 1/8W-S	R17	$300.99 k \Omega$	$\pm 8000V$	$300.99 k \Omega$
	RM1206 301.0kΩ 0.1% 1/8W-S	R18	$30.995 \mathrm{k}\Omega$	$\pm 8000V$	$30.995 k\Omega$
	RM1206 301.0kΩ 0.1% 1/8W-S	R19	$301.06 k\Omega$	±8000V	$301.06 k\Omega$
	RM1206 301.0kΩ 0.1% 1/8W-S	R20	$301.05 k\Omega$	±8000V	$301.05 \mathrm{k}\Omega$

<u>NOTE</u>: Resistor R4 was de-capped after simulation study and optical photograph revealed internal resistive pattern are melted and partially discontinued at certain location due to electrical overstress (refer figure-7). However, this signature is not similar to moisture induced corrosion related failure.



Figure-7: Localized Melting of Resistive Tracks of the Degraded Resistor R4



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# C. Electrostatic Discharge (ESD) Simulation Study on Die/Wire Bondable Type Thin Film Chip Resistors RM1206, 0.1%, 25PPM, 1/8W (Few Values)

Die/wire bondable type thin film resistors are being used in HMCs [10][11], wherein few resistors failed in open mode during screening/qualification test. Construction of die type thin film chip resistors is different from that discrete type thin film chip resistors. Die type chip resistors are silicon base, whereas, discrete type thin film chip resistors are ceramic (Al $_2$ O $_3$ ) based. However, in both cases, the resistive element is same i.e., Nichrome thin film. After studying the ESD induced failure mechanism in discrete type thin film chip resistors, it was intended to understand the failure mechanism in die type thin film resistors w.r.t. ESD.

a. Initial Visual Examination and Electrical Measurement of Chosen Components:

Few die type thin film resistors of different values were chosen for the study. Details about the components are shown in table-7.

TABLE-7: Components Details Taken for Simulation Study

Resistance Value	Sample Nos.	Sample Marking
100Ω±0.1%	3nos.	R1 to R3
1.5kΩ±0.1%	3nos.	R4 to R6
12.0kΩ±0.1%	3nos.	R7 to R9
22.0kΩ±0.1%	3nos.	R10 to R12
56.0kΩ±0.1%	3nos.	R13 to R15
100.0kΩ±0.1%	3nos.	R16 to R18
240.0kΩ±0.1%	3nos.	R19 to R21
470.0kΩ±0.1%	3nos.	R22 to R24

**NOTE:** Chip resistors dice were visually inspected using optical microscope at 100X. No visual anomalies were observed.

## b. ESD Simulation Study by Step Stress Method:

To understand the effect of ESD on die type thin film chip resistors, ESD simulation study was carried out by mounting the aforesaid resistor dice in 48 pins metallic HMC package and ESD pulses were applied between the HMC pins, which were connected internally to the pads of chip resistor dice. ESD pulses were applied with Human Body Model ESD simulator as per MIL-STD-883K method 3015.7. ESD pulses were applied with Human Body Model ESD simulator as per MIL-STD-883K method 3015.7. ESD pulses were applied by step stress method in a step of  $\pm 250$ V starting from  $\pm 500$ V. However, a final applied ESD pulse is shown in the table for the sake of brevity. Pre and post-ESD resistance measurement was carried out on the chip resistors and the obtained test results are shown in table-8.

**Table-8: ESD Simulation Study Result** 

Resistor Sl. No.	Initial Value of Resistors	Applied ESD Pulses	Final Value of Resistors	Remarks	
R1	99.98Ω	±500V,5pulses	99.98Ω	E-:1-4: O4-	
R2	$99.97\Omega$	±750V,5pulses	$99.97\Omega$	Failed in Open mode (Figure-8)	
R3	$100.03\Omega$	±1000V,5pulses	Open	(Figure-6)	
R4	$1.498$ k $\Omega$	±500V, 5pulses	1.498kΩ	Eailad in Onan mada	
R5	1.501kΩ	±750V, 5pulses	$1.501$ k $\Omega$	Failed in Open mode (Figure-9)	
R6	1.499kΩ	±1000V,5pulses	Open	(Figure-9)	
R7	11.998kΩ	±500V, 5pulses	11.998kΩ	Eailad in Onan mada	
R8	11.999kΩ	±750V, 5pulses	11.999kΩ	Failed in Open mode (Figure-10)	
R9	$11.997k\Omega$	±1000V,5pulses	Open	(Figure-10)	
R10	21.998kΩ	±500V, 5pulses	21.998kΩ	E-:1-4: O4-	
R11	$22.002k\Omega$	±750V, 5pulses	$22.002k\Omega$	Failed in Open mode (Figure-11)	
R12	$21.997k\Omega$	±1000V, 5pulses	Open	(Figure-11)	
R13	55.998kΩ	±500V, 5pulses	55.998kΩ		

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Failed in Open mode	55.999kΩ	±750V, 5pulses	55.999kΩ	R14
(Figure-12)	Open	±1000V,5pulses	55.999kΩ	R15
Eailad in Onan mada	$301.003k\Omega$	±1000V,5pulses	99.999kΩ	R16
Failed in Open mode (Figure-13)	$300.997k\Omega$	±1250V,5pulses	99.998kΩ	R17
(Figure-13)	Open	±1500V,5pulses	99.999kΩ	R18
E-:1- 4 : O 4-	239.999kΩ	±1000V,5pulses	239.999kΩ	R19
Failed in Open mode (Figure-14)	$240.002k\Omega$	±1250V,5pulses	$240.002k\Omega$	R20
(Figure-14)	Open	±1500V,5pulses	$239.998k\Omega$	R21
Eailad in Onan mada	999.998kΩ	±1500V,5pulses	999.998kΩ	R22
Failed in Open mode (Figure-15)	999.999kΩ	±1750V,5pulses	999.999kΩ	R23
(Figure-15)	Open	±2000V,5pulses	999.999kΩ	R24

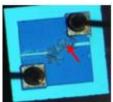


Figure-8: Discontinuity of thin Film track of resistor R3



Figure-9: Discontinuity of thin Film track of resistor R6



Figure-10: Discontinuity of thin film track of resistor R9



Figure-11:
Discontinuity of thin film track of resistor
R12

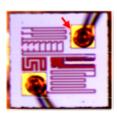


Figure-12: Discontinuity of thin film track of resistor R15

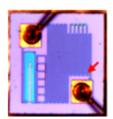


Figure-13: Discontinuity of thin film track of resistor R18

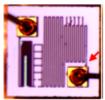


Figure-14:
Discontinuity of Thin
Film Track of
Resistor R21

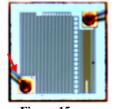
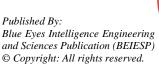


Figure-15: Discontinuity of Thin Film Track of Resistor R24

#### IV. RESULTS AND DISCUSSION

As discussed in section-A, Electrical Overstress (EOS) simulation study was conducted on discrete type thin film chip resistors RM1206, 0.1%, 25PPM, 1/8W.





## A Comprehensive Study on Failure Modes and Mechanisms of Thin Film Chip Resistors

From EOS simulation study, it was inferred that the simulated resistors failed in open mode with application of voltage >twice the rated voltage (100V). Before open mode failure, resistance of the resistors appreciably increased. In this case, resistor pattern got distorted at certain location due to high dissipation, which resulted in increase in resistance value, but complete open mode failure was not observed. Failure mechanism in this case can be described as joules heating effect. This failure mechanism is not similar to that of manual soldering simulation explained in section-2, wherein resistor pattern near end cap region of chip resistor got completely eroded as a result of moisture/contaminant induced corrosion. Therefore, failure signature in chip resistor RM1206 as a result of manual soldering simulation did not match with that of EOS simulation.

As discussed in section-B, ESD simulation study was conducted on discrete type thin film resistor RM1206, 0.1%, 25PPM, 1/8W. From ESD simulation study, it is inferred that these types of resistors are not very sensitive to ESD. Only lower value resistors ( $10K\Omega$  and  $20K\Omega$ ) are susceptible at 6000V to 7000V ESD pulses, whereas higher value resistors  $(>20k\Omega)$  did not show any susceptibility to ESD. Internal visual signature of ESD stressed chip resistor indicated localized distortion of resistive tracks at few locations, which is similar to that of EOS induced failure with same failure mechanism i.e., joules heating effect. Also, ESD induced resistors are failing in higher resistance mode not in complete open mode, which is also similar to that of EOS induced failures. As discussed in section-C, ESD simulation study was conducted on die type thin film resistor. From ESD simulation study, it is inferred that these types of resistors are very sensitive to ESD, wherein, the resistive thin film track got opened/discounted. Resistors values ≤55kΩ failed in open mode with ESD stress ≥1000V. Whereas higher value resistors failed with higher ESD stress such as 1500V and 2000V. Therefore, die type thin film resistors can be classified as class-1 ESD sensitive devices. Even though the resistive elements for both discrete type and die type thin film resistors are same i.e. Nichrome, the difference between them is their substrate. Discrete type thin film resistors have ceramic (alumina) substrate, whereas die type thin film resistor have silicon substrate. This indicates that ESD sensitivity of silicon based thin firm resistor is more than that of alumina based thin firm resistor. The reason behind the above observation could be probably due to higher electrical conductivity of silicon (~1.67x10<sup>-2</sup> mho/cm), in comparison to that of ceramic (Alumina) (~10<sup>-14</sup>mho/cm). Because of higher electrical conductivity of Silicon, ESD pulse discharges un-disruptively thorough Silicon die by damaging the thin film resistive element. The same mechanism does not applicable to ceramic based thin film resistor because the ESD pulses disrupted and dissipated on the lesser conductive surface. However, more study is needed to understand the ESD sensitiveness of die type thin film resistors.

### V. CONCLUSION

Controlled experiments were conducted to demonstrate effect of EOS and ESD on discrete type thin film resistor (RM1206 chip resistor, 0.1%, 25PPM, 1/8watt). From the study, it was understood that EOS simulated resistors failed in open mode with application of voltage >twice the rated voltage (100V), wherein, resistor pattern got distorted at certain location due to high dissipation, which resulted in

increase in resistance value, but complete open mode failure was not observed. Similarly, from ESD simulation study, it is inferred that these types of resistors are not very sensitive to ESD. Only lower value resistors ( $10K\Omega$  and  $20K\Omega$ ) are susceptible at 6000V to 7000V ESD pulses. Internal visual signature of ESD stressed chip resistor indicated localized distortion of resistive tracks at few locations, which is similar to that of EOS induced failure. Also, ESD induced resistors are failing in higher resistance mode not in complete open mode, which is also similar to that of EOS induced failures. Controlled ESD simulation study on die type chip resistors has a different type of observation. From ESD simulation study, it is inferred that these types of resistors are very sensitive to ESD, wherein, the resistive thin film track got opened/discounted. Resistors values  $\leq 55k\Omega$  failed in open mode with ESD stress ≥1000V. Whereas higher value resistors failed with higher ESD stress such as 1500V and 2000V. Therefore, die type thin film resistors can be classified as class-1 ESD sensitive devices. Even though the resistive elements for both discrete type and die type thin film resistors are same i.e. Nichrome, ESD sensitivity is different for both. Reason for the above reason could be explained in terms of conductivity of their base substrate, further experiment is under progress for in depth understanding.

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Authors Contributions	All authors have equal participation in this article.

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