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# Interval Type - 2 Fuzzy Logic Controller Based Shunt Active Power Filter for Power Quality Enhencement

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***Abstract:** Frequent widespread use of power electronics equipment by consumers has led to power quality problems in the power system network, due to their nonlinearity. Due to this problem, the current and voltage waveforms are no longer sinusoidal, resulting in the generation of harmonics. Various methods have been deployed to mitigate harmonic issues, including passive power filters and shunt active power filters. Presently, passive power filters are limited in use because of their demerits, including the production of parallel resonances, being heavy in size, and mitigating only a few harmonics. With the advancement in technology, shunt active power filters have become superior to passive power filters due to their limitations. Shunt active power filters were tested for suppressing harmonics produced by nonlinear loads. This article uses a synchronous reference frame (SRF) in generating harmonics produced by nonlinear loads. However, T2FLC is used to control the DC bus voltage of the filter constant. A hysteresis current controller was introduced to fire the gating signal of the IGBT inverter circuit. MATLAB software was deployed in the simulation work. Results obtained have satisfied the tolerable 2014 revised harmonics limit.*

***Keywords**: SRF, Harmonic Issues, T2FLC*

## I. INTRODUCTION

Due to the high increase in population worldwide, the demand for energy and electricity sources is imperative for the teeming population. With these, more generations, transmission, and distribution networks are needed to meet the demand. However, the widespread use of modern electronics devices by consumers has led to the problem of harmonic distortion and power quality issues[1][2]. The solutions to the harmonic distortion are the filters, which will significantly reduce the issues of imbalance on the power systems [3]. Classical passive power filters were used to mitigate current harmonic distortions caused by nonlinear loads; however, passive filters have several disadvantages, including being heavy and bulky in size, as well as exhibiting series and parallel resonances. That is why they are not in much service nowadays. Now, shunt active power filters are superior to traditional power filters, which have been proven and tested to be the viable solution to mitigate current harmonic distortion to overcome the problem of passive power filters[4]. The reason why shunt active power filters are used rather than passive power filters is because of their superior characteristics, like complete mitigation of harmonics and reactive power compensation [5]. Various methods are used to control the gating signals of the IGBT/MOSFET inverter circuit, including Pulse Width Modulation, Hysteresis current controllers, and sliding mode controllers.

It is well known that the Fuzzy Logic system was adopted by Zadeh in 1965[6]. With the introduction of Fuzzy, many researchers have developed an interest in designing Fuzzy Logic Controllers for various engineering applications. However, with development in research, a lot of researchers have put more interest in (T2FLC), which was initiated by L. Zadeh due to uncertainties and nonlinearities with the type-1 Fuzzy Logic controller (T1FLC). (T1FLC) and (T2FLC) are almost identical in design, differing only in the type of reduction block used in (T2FLC). The footprint of uncertainty (FOU) is a key feature of T2FLC, indicating the level of uncertainty and nonlinearity within the system. (T2FLC) is more robust in dealing with uncertainty when correlated with (T1FLC)[7][8] Frequent use of the (PI) and (PID) controllers is used to maintain the DC bus voltage regulation of the SAPF [9]

For this article, T2FLC is proposed to maintain the DC bus voltage constant for the SAPF. Section 2 discusses the concept of extracting current harmonic distortion using synchronous reference frame (SRF) d-q theory. In contrast, Section 3 describes the hysteresis current controller (HCC), and Section 4 explores the design of the T2FLC. While Section 5 presents the simulation results and analysis, the conclusion and references are provided at the end of the paper.

## II. REFERENCE CURRENT EXTRACTION TECHNIQUES

The time domain is utilised for extracting the harmonic current through a simple mathematical computation, and the technique provides precise detection of both different and duplicate harmonic load currents. However, the advantage of this approach is that it yields a quick result compared to other techniques. This method is a time-domain-based algorithm that aims to generate a harmonic current capable of performing in dynamic state conditions, thereby controlling the filter perfectly when developed as a real-time application.

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However, SRF theory has another feature of simplicity of mathematical computation, which involves only algebraic calculation [10].

Figure 1 depicts the classical SRF block diagram. The basic structure of the algorithm utilises a Phase-Lock-Loop (PLL) circuit specifically for synchronisation.

In this algorithm, the load currents of the line currents $i_{La}$, $i_{L_b}$ and $i_{Lc}$ They are in stationary axis coordinates, which are converted into two-phase, the direct axis (d) and quadrature axis (q) rotating coordinates, and currents $i_d - i_q$ As given in matrix notation:

$$\begin{bmatrix} i_d \\ i_q \end{bmatrix} = \frac{2}{3}\begin{bmatrix} \sin\theta & \sin\left(\theta-\frac{2\pi}{3}\right) & \sin\left(\theta+\frac{2\pi}{3}\right) \\ \cos\theta & \cos\left(\theta-\frac{2\pi}{3}\right) & \cos\left(\theta+\frac{2\pi}{3}\right) \end{bmatrix}\begin{bmatrix} i_{La} \\ i_{Lb} \\ i_{Lc} \end{bmatrix} \quad (1)$$

The generated reference frame is rotating synchronously with the fundamental currents. Moreover, the time-variant currents, together with the basic frequencies, are kept nearly steady after conversion. The d-axis current components are intentionally designed to remove harmonics and the reactive components of the power. But the d-q transformation output signals rely on the load current and the action of the phase locked loop[11]

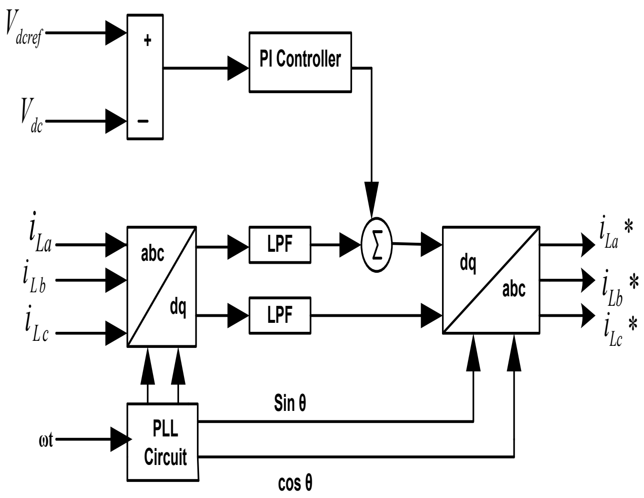


**Figure 1. Synchronous Reference Frame**

The components of the $i_d - i_q$ Currents were filtered to remove the superior-order harmonic components, allowing the main frequency components to remain. The PI controller is purposely designed to eliminate the steady-state error of the DC component. The positive sequence fundamental frequency of the active components of the $d-q$ Currents are added to reduce losses in the inverter by maintaining the d. c. voltage constant or within a limit. However, the resultant current $(a-b-c)$ The stationary frame is also determined from $i_d - i_q$ Rotating frame using the second transformation.

$$\begin{bmatrix} i_{sa}* \\ i_{sb}* \\ i_{sc}* \end{bmatrix} = \begin{bmatrix} \sin\theta & \cos\theta \\ \sin\left(\theta-\frac{2\pi}{3}\right) & \cos\left(\theta-\frac{2\pi}{3}\right) \\ \sin\left(\theta+\frac{2\pi}{3}\right) & \cos\left(\theta+\frac{2\pi}{3}\right) \end{bmatrix}\begin{bmatrix} i_d \\ i_q \end{bmatrix} \quad (2)$$

The generated current from the SRF algorithm is correlated with the main currents and also produces the targeted switching pulses for the inverter using a hysteresis current controller. Similarly, the PLL circuit is referenced to the source voltage for vector orientation.

## III. HYSTERESIS CURRENT CONTROLLER

This type of controller is also referred to as a fixed (HCC) controller, which is used to switch the gating signals of the inverter.

The classical hysteresis current controller works with an inverter by differentiating the current error e(t) with a fixed hysteresis limit. Figure 2 (a) depicts the block diagram of HCC. The difference between the reference current and primary current gives rise to a current error. If the current exceeds the upper limit of the hysteresis limit, the upper switch of the inverter arm is OFF and the bottom switch is ON, due to that, the current starts to reduce [12]. However, Figure 2(b) depicts the switching pattern used to drive the inverter into ON and OFF modes. However, if the error current exceeds the bottom limit of the band, the bottom switch is in the OFF position, and the upper switch is in the ON position. Due to that, the current returned to the hysteresis band position. Additionally, the primary current is now directed to search for the reference current within the hysteresis limit. In this work, HCC is proposed due to its simplicity in implementation.

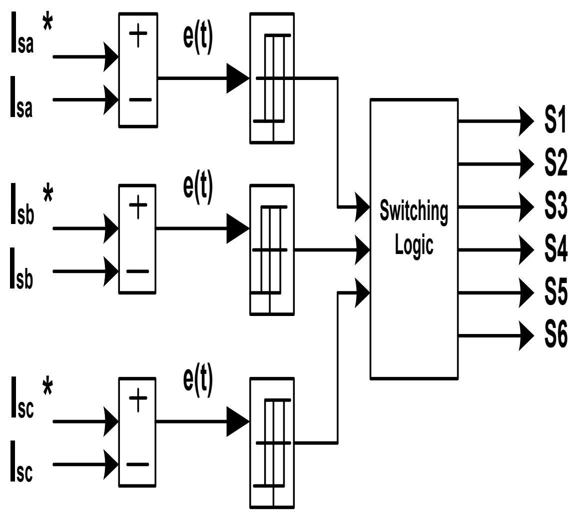


**Figure 2(a). Hysteresis Current Controller Switching Pattern**

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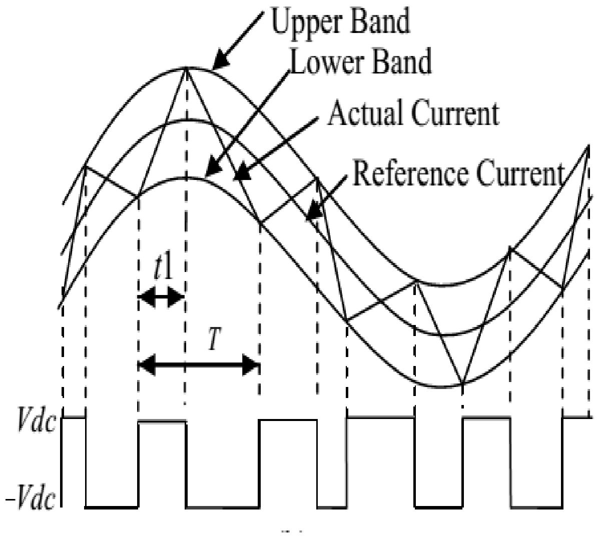


**Figure 2(b). Hysteresis Current Controller [13]**

A typical example of phase-A switching performance is given by the expression:

$$S=OFF \text{ if } i_{sa}(t) > i_{sa}{\times}(t) + hb \quad (3)$$
$$S=ON \text{ if } i_{sa}(t) < i_{sa}{\times}(t) - hb$$

A two-level hysteresis current controller is employed in the shunt filter due to its simplicity in implementation. This controller only employed the use of a DC supply voltage to produce the pulses of the inverter [14].

## IV. T2FLC

L. Zadeh first developed a Type-2 Fuzzy Logic controller to solve the uncertainties with the traditional Type-1 fuzzy logic controller [15]. The design structure of T2FLC is similar to that of Type 1FLC, with only a different type of reduced block in T2FLC. However, a type-2 fuzzy set is represented by Ā, which is also described as:

$$\breve{A} = ((y, u), \mu_A(y, u)) I \ \forall_x \in X \quad (4)$$

Where X is the input variable domain and y is the range of the input variable, u is the primary grade of the type-2 fuzzy logic set, and $J_x$ Is the membership of T2F set, and $\mu_A(x,u)$ It is the secondary membership of the fuzzy set. So, T2F, which denotes a continuous universe of discourse, is described in Equation 5 below.

$$A^2 = \int_{x\in X} \int_{u\in Jx} uA(x,u)/(x,u) \quad (5)$$

Here, $J_x \subseteq [0,1]$ and $\iint$ Represent the union on all the values of $x$ and $u$ . However, $A$ Can be written as:

$$A = \left(x, \mu_A(x)\right) / \forall \in X \quad (6)$$

$$A = \int_{x\in X} \left[ \int_{u\in J_X} f_x(u)/u \right] / xJ_X \subseteq [0,1] \quad (7)$$

$$A = \sum_{i=1}^{N} \left[ \sum_{u\in J_{xj}} f_{xj}(u)/u \right] / x_i \quad (8)$$

The membership union is referred to as the Footprint of Uncertainty (FOU). Also, (FOU) is denoted mathematically as:

$$\text{FOU}(A) = \bigcup_{x\in X} J_x \quad (9)$$

The basic structure of T2FLC is similar to the classical T1FL structure, with only differences in the type reduction block of the type-2 fuzzy logic controller. Figure 3. Depicts the structure of T2FLstructure.

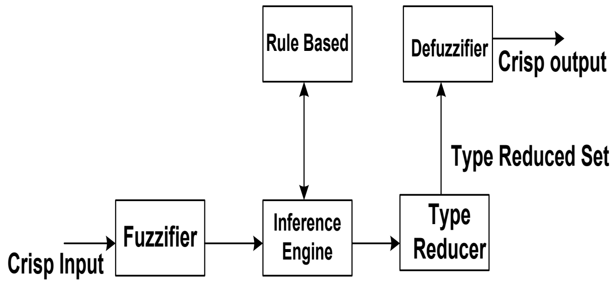


**Figure 3. T2FLC Block Representation**

However, T2F, each membership grade is fuzzy itself, ranging between (0, 1), unlike in a type-1 fuzzy system, where the memberships are only crisp numbers (0, 1) [16].

- Fuzzification process: The fuzzification is the input blocks that received and processes the crips values and processes it in to the inference engine for onward processing.
- Knowledge Base: The block aims to define the linguistic terms for the two inputs and single output, specifically for error and change of error, respectively.
- Inference Mechanism: This block accepts the fuzzified crisp values and rule base, which further results in the type reduction block for the defuzzification process.
- Type reduce block: The type reduction block is aimed at converting the crisp value into a type-1 fuzzy set before the fuzzification process.
- Defuzzification process that is responsible for converting the fuzzified output data, as determined by the output membership functions, into the control system that is to be controlled.

**Table 1 Rule Table**

| E | N | Z | P |
|---|---|---|---|
| **N** | N | LN | Z |
| **Z** | LN | Z | LP |
| **P** | Z | LP | P |

Table 1. Shows the rule table of the T2FLC, which defines the linguistic rules as: Error (E), Change of error (CE), Negative (N), Positive (P), Zero (Z), Large Negative (LN), and Large Positive (LP).

### A.Simulation Studies

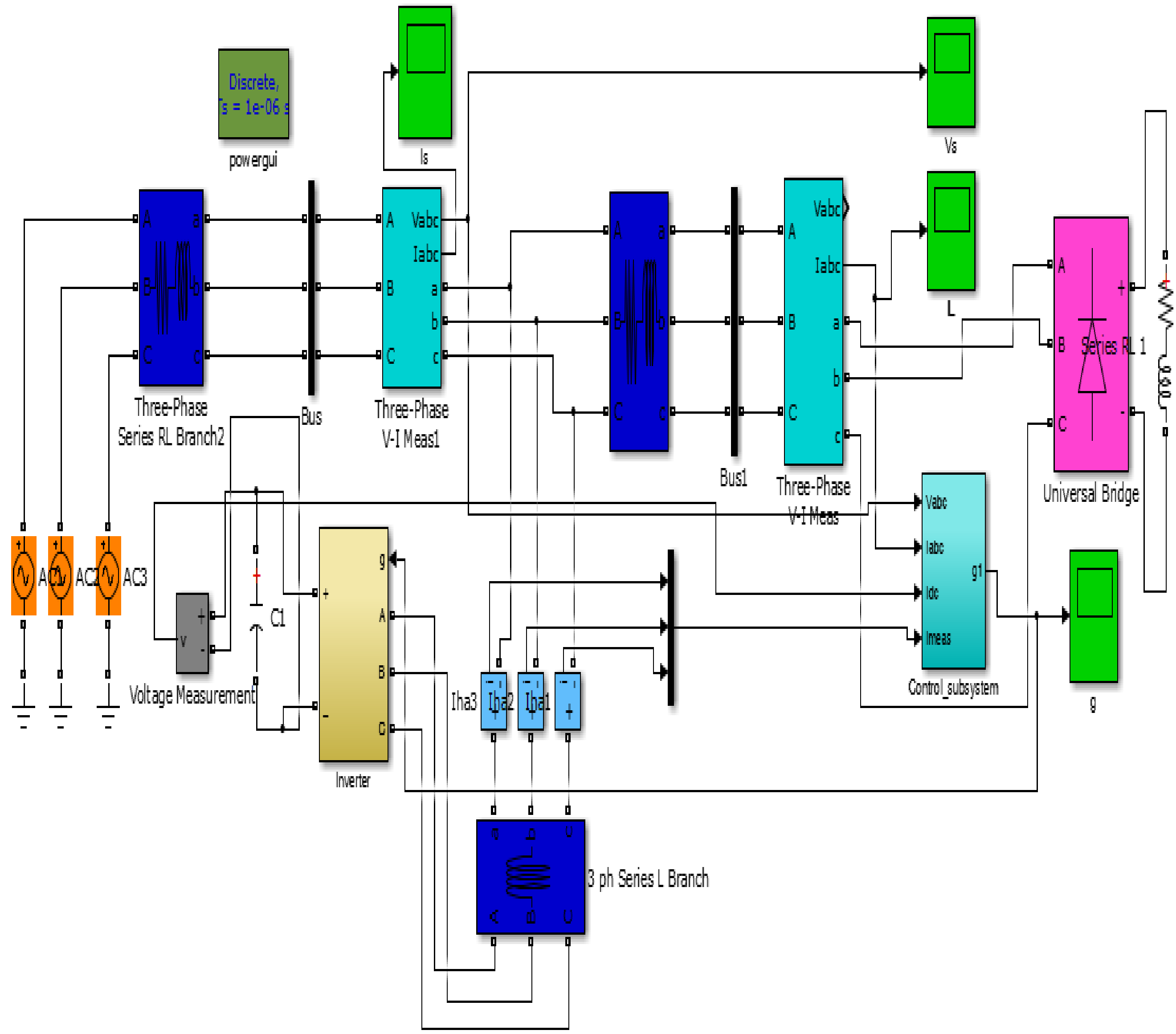


**Figure 4. Complete SIMULINK of Shunt Active Power Filter**

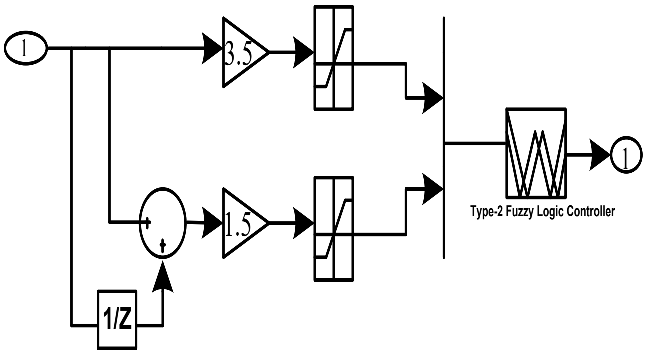


**Figure 5. Subsystem of the Simulink Model of T2FLC**

Figure 4. Shows the complete simulation work using MATLAB/SIMULINK—the extraction technique using synchronous reference frame, the T2FLC.

Moreover, Figure 5 depicts the subsystem of the T2FLC, which has two inputs: error (E) and its derivative (ΔE), with a single output.

### B. Simulation Results and Analysis

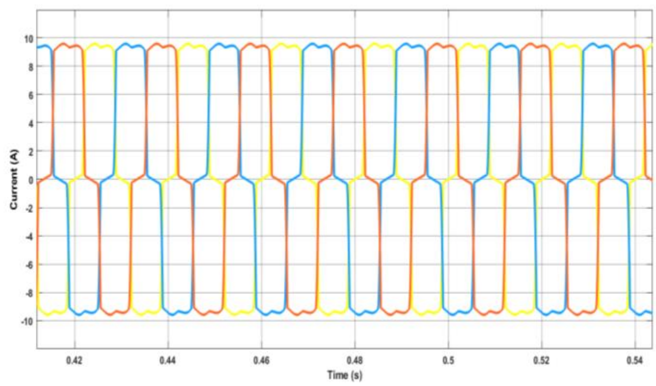


**Figure 6. Load Current Before Compensation with Filter**



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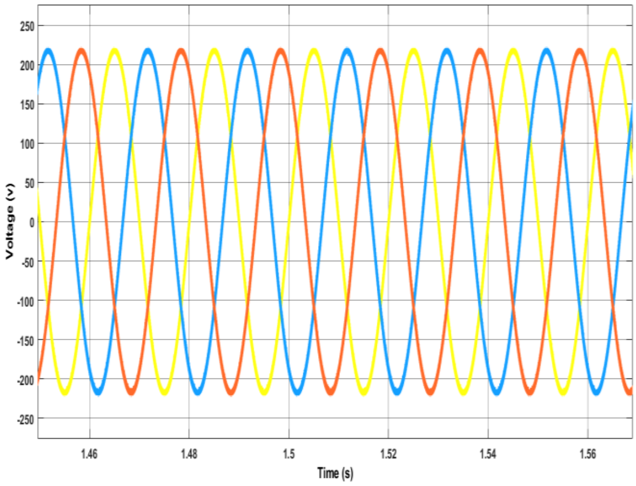


**Figure 7. Source Voltage**

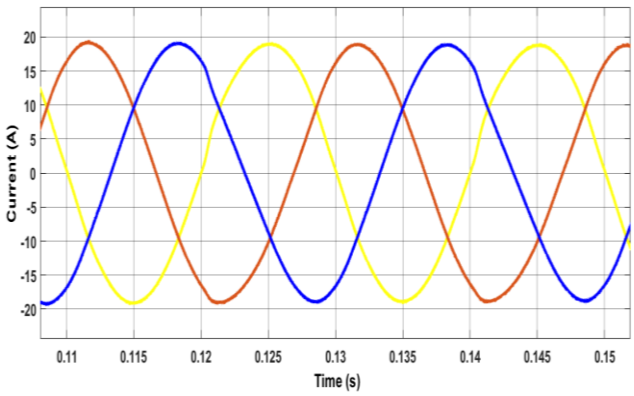


**Figure 8. Source Current After Compensation Filter**

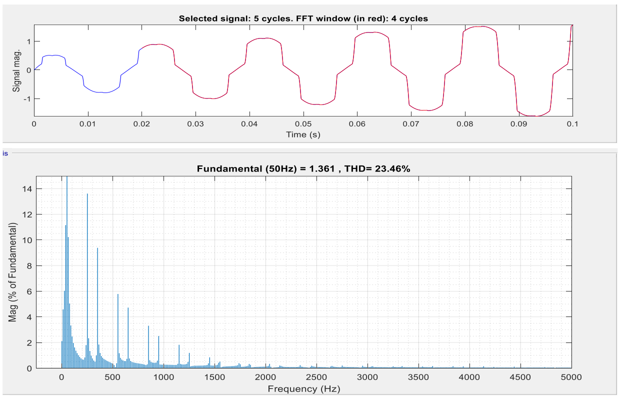


**Figure 9. Total Harmonic Distortion (THD%) before applying filter.**

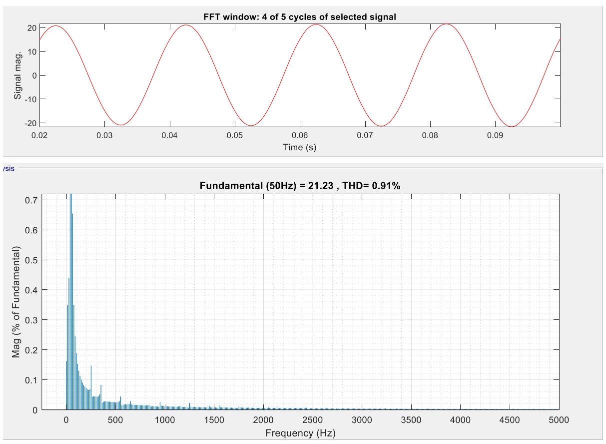


**Figure 10. Source Current after applying the filter.**

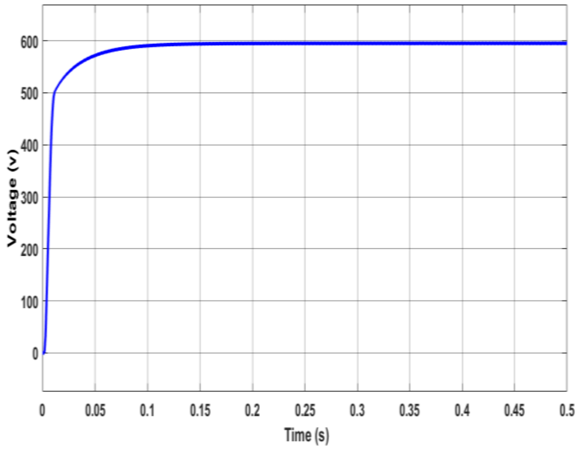


**Figure 11. D.C Bus Voltage of the Filter**

Figure 6. Shows the load current due to a nonlinear load without using the SAPF. While Figure 7. Is the supply voltage, which is supposed to be purely sinusoidal, even with or without applying the filter? Figure 8. Depicts the supply current after applying the filter and is in the same polarity as the supply source voltage. Moreover, Figure 9. Shows the level of harmonic distortion using Fast Fourier Transform, and the THD% found to be 23.46% which did not satisfy the imposed IEEE 519-2014 norms. Figure 10 shows the compensated current after applying the SAPF, with a THD% of 0.91%, which fulfils the recommended harmonic norms; meanwhile, Figure 11 shows. Indicate the stability of the direct current bus voltage, which stabilised at 600V.

## V. CONCLUSION

A design simulation of a SAPF with T2FLC for improving power quality was achieved in the article. The results obtained for the THD% of the load current and supply current were 23.46% and 0.91%, respectively, without and with the shunt active power filter active. These results demonstrate the filter's capability to mitigate the harmonics produced by nonlinear loads, and the results obtained satisfy the required IEEE harmonic norms. However, the controller has demonstrated its effectiveness in reducing harmonics to their minimum level.

## DECLARATION STATEMENT

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| Authors Contributions | All authors have equal contributions to this article. |

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