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Design and Performance Analysis of Non-Volatile Adder Using Magnetic Tunnel Junction (MTJ)

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Abstract: ***This paper discusses the design of the proposed precharged high DCSL MTJ full adder, the proposed precharged low DCSL MTJ full adder & proposed improved precharge low DCSL MTJ full adder, utilising several methodologies in this study. The designs were simulated using the LTspice XVII software. Results indicate that the proposed precharge DCSL MTJ-based complete adder architecture consumes less power than other full adder architectures. In comparison to other complete adders, it also needs fewer transistors. Therefore, it is adequate to develop a non-volatile serial adder utilising MTJ using the MTJ-based complete adder. Non-volatile serial adder circuits now require a high supply voltage (Vdd) for both writing and sensing operations, which is an energy-intensive process. Scaling down Vdd is a valuable technique for reducing dynamic power consumption in low-power electronic devices, thereby satisfying the power budget. The average power consumption and Average delay of the Proposed improved precharge low DCSL MTJ full adder are 39.53 pW & 1.90 fs, respectively.***

Keywords: DCSL, MTJ, FSM, STT, AP, RAM, Precharged

I. INTRODUCTION

The adder is one of the most essential logic components used in the design of digital VLSI circuits. The fundamental operation in mathematics is addition [1]. It is the foundation for practically all calculations, including multiplication, counting, and filtering. In addition to completing addition tasks, its principal function, the adder also acts as an essential component in various intricate circuits, such as multipliers, subtractors, RAMs, and address computations, among others [2], [3]. The rapid development in transistor count on circuits has dramatically improved the performance of computer systems.

Non-volatile serial adders are necessary in a finite state machine (FSM). This suggests that the input value and strength will significantly determine the subsequent state, thereby improving the performance of the compound system.

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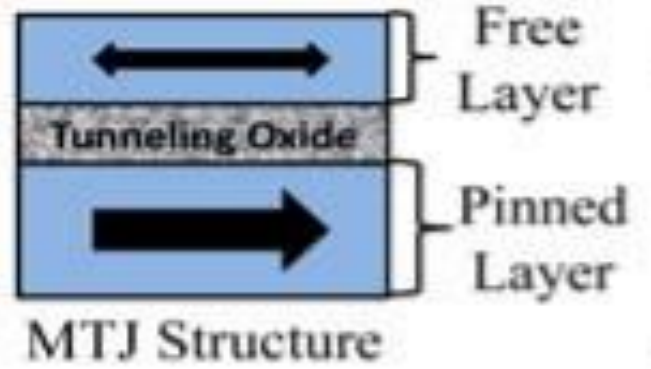
Essentially, there are two primary approaches to setting up a sequential logic design: Mealy machines and Moore machines. FSM is a computational model that can be run on hardware or software. Sequential logic and a few computer programs are developed using this. FSMs solve issues in various fields, including mathematics, artificial intelligence, games, and linguistics. When specific inputs can cause exact state changes that FSMs can indicate in a system. The outputs of the perpetual serial adder, a Mealy state machine, depend on the inputs and states at every given moment. The mealy state machine block diagram represents memory and combinational logic components. The machine's memory may contain several of the previously mentioned outputs that can be used as inputs to combinational logic.

The non-volatile serial adder (also known as a binary serial adder) comprises a complete adder circuit, shift registers, and a flip-flop, which performs addition in serial form [4] [11].

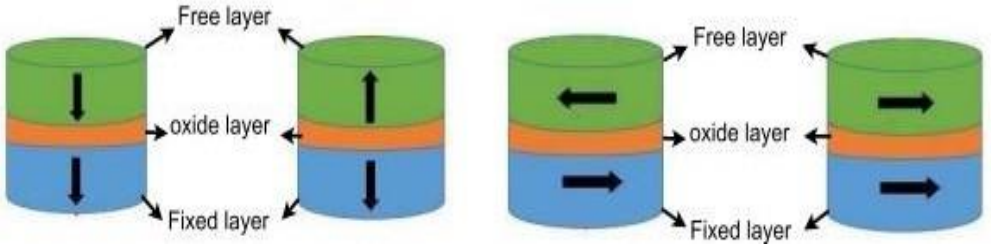
The motivation for conducting this research is to ensure that any electronic device is reliable and trustworthy. The components inside it play an essential role. One such complex circuit is the non-volatile serial adder. Thus, we decided to work on it and improve the existing proposed circuits by applying the newly advanced techniques and methods. The writing and sensing operations of non-volatile serial adder circuits require a high supply voltage (Vdd), which consumes a significant amount of energy. Scaling down Vdd is an efficient way to reduce the dynamic power consumption of low-power electronic devices, thereby satisfying the power budget. Nevertheless, lowering Vdd causes leakage power to rise. Moreover, the efficiency of Vdd scaling has decreased to the point where additional Vdd reduction causes improper circuit operation or a drop in the circuits' energy efficiency [5].

II. MAGNETIC TUNNEL JUNCTION

Magnetic tunnel junctions (MTJs) are nanostructured devices within the field of magneto-electronics, also known as spin electronics [6], [7], and subsequently referred to as spintronics [8], [9] [10]. As shown in Figure 1, the MTJ comprises two ferromagnetic layers (FM), one fixed and the other free, separated by an oxide barrier layer. The FM layer in an MTJ device can be oriented either parallel or antiparallel to the magnetisation direction. Depending on whether the FM layers are parallel (P) or antiparallel (AP) (as shown in Figure 2), the MTJ device exhibits either low resistance (RP) or high resistance (RAP) characteristics. Spin transfer torque (STT) is a proposed method of reversing the magnetisation orientation of the free layer, which enables the creation of highly reliable MTJ/CMOS hybrid circuits that consume less power.



[Fig.1: Structure of MTJ]



[Fig.2: (a) Parallel and (b) Antiparallel Structure of MTJ [5]]

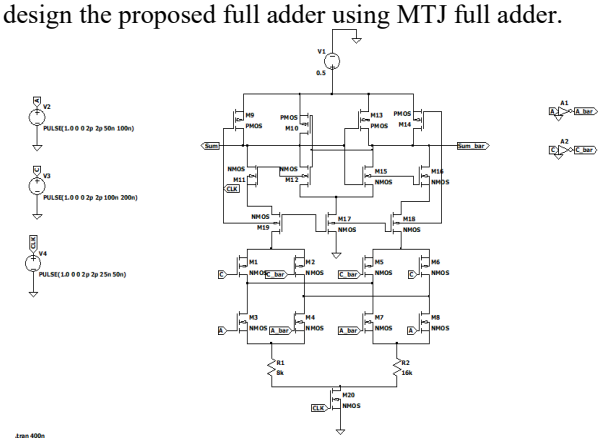
The existing system has the disadvantage of high-power consumption and power leakage, which in turn reduces the device's efficiency. Additionally, the system operates at a comparatively low speed. Due to power leakage, the system's lifetime is also decreased. Numerous academics have Attempted to construct ever-more-efficient non-volatile serial adders considering recent technological advancements. Most signal processing techniques include addition as a fundamental function. The current system utilises a low-power D-Flip-Flop serial adder. The entire adder circuit and MTJ will be utilised in the system proposed in this study (Magnetic Tunnel Junction [12]). Depending on the resistance that becomes parallel or anti-parallel, as well as the orientation, the spin transfer torque (STT) MTJ, which stores binary bits 0 or 1, will be used. Since the MTJ has almost zero power leakage and the old system's power consumption is also decreased, the primary issue of power leakage in the system is resolved [13]. The system is relatively fast and efficient compared to the current system. Additionally, the proposed system has a longer lifespan.

III. RESULTS AND DISCUSSION

In this paper, to implement the non-volatile adder, we analysed the full adder and understood the power consumption and the area required to design it. We then implemented a static CMOS full adder using the LTspice software and measured the power consumption and delay of the output. The design will be implemented using 45 nm technology, and the transistors needed to create a complete adder will be recorded. After that, a dynamic full adder circuit is implemented, and the output delay and power consumption are determined. The differential cascade voltage switch logic (DCVSL) full adder will next be designed, and the output's power usage and latency will be evaluated [14]. The DVCSL complete adder will be created using 45nm technology, and the required number of transistors will be recorded. The full adder, which utilises the MTJ, is developed using an efficient technique that consumes minimal power and space. Since the MTJ that we utilise for the design exhibits the properties of a resistor, we will opt for a resistor instead. We will design the non-volatile serial adder using MTJ and examine the power usage and latency after studying the whole adder using MTJ.

A. Proposed Precharge High DCSL MTJ Full Adder:

The proposed precharged high DCSL comprises precharged transistors, a cross-coupled inverted pair, and an NMOS evaluation tree. When the gate is first operating, the output nodes are charged high and CLK low. When the NMOS tree has steady inputs and the CLK is high, the gates assessment process starts. The precharge high DCSL is used to design the proposed full adder using MTJ full adder.



[Fig.3: The Design of Proposed Precharge High DCSL Whole Adder Sum Circuit in LTspice]

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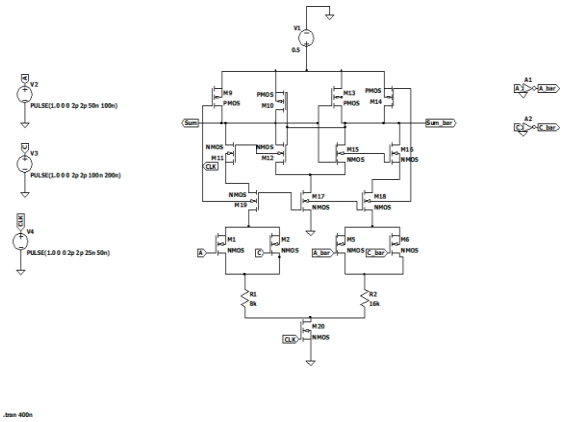


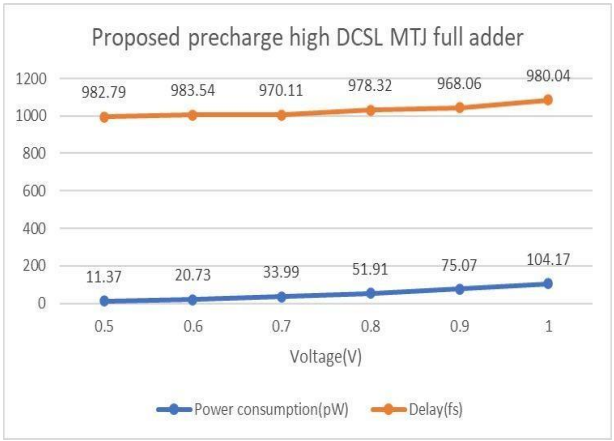
[Fig.4: The Design of Proposed Precharge High DCSL Full Adder Carry Circuit in LTspice]

B. The Output of the Proposed Precharged High DCSL MTJ Full Adder

Table I: Showing the Power Consumption and Delay of Proposed Precharge High DCSL MTJ

Voltage(V)	Power Consumption(pW)	Delay(fs)
1	104.17	980.44
0.9	75.07	968.06
0.8	51.91	978.32
0.7	33.99	970.11
0.6	20.73	983.54
0.5	11.37	982.79

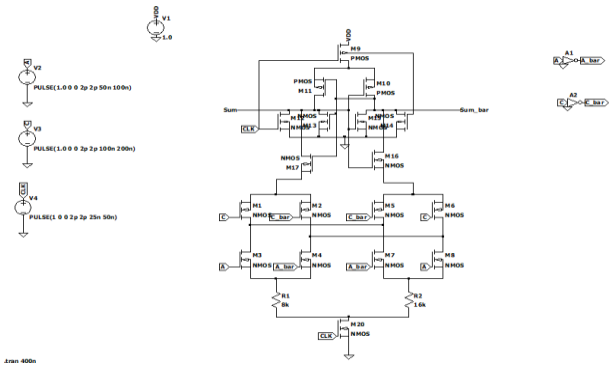
Table 1 presents the power consumption (pW) and delay (fs) of the proposed precharged high DCSL MTJ full adder at various voltages, ranging from 0.5 V to 1.0 V. It can be observed that the power consumption increases with increasing voltage. In contrast, the delay remains relatively constant, with only slight changes.



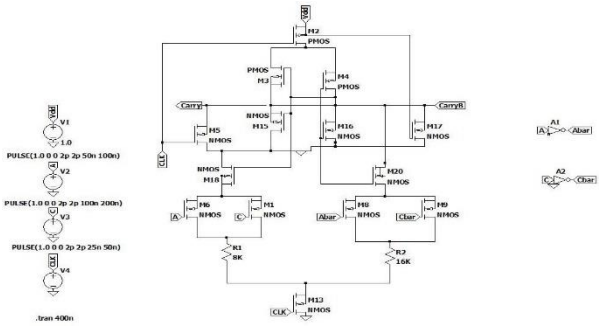
[Fig.5: Graph Showing the Power Consumption(pW) and Delay(fs) of Proposed Precharge High MTJ Full Adder at Different Voltages (V)]

C. Proposed Precharge Low DCSL MTJ Full Adder

The power consumption and delay are high; therefore, the proposed precharge high DCSL MTJ complete adder logic with outputs precharged is modified to have outputs charged low. The circuit evaluation takes place when CLK goes high. Thus, we propose a Precharge low DCSL MTJ full adder to overcome the high-power consumption and delay.



[Fig.6: The Design of Proposed Precharge Low DCSL Whole Adder Sum Circuit in LTspice]



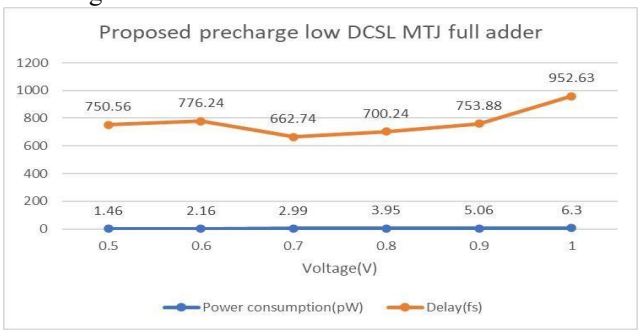
[Fig.7: The Design of Proposed Precharge Low DCSL Full Adder Carry Circuit in LTspice]

D. The Output of the Proposed Precharged Low DCSL MTJ Full Adder

Table II: The Power Consumption and Delay of Proposed Precharge Low DCSL MTJ Full Adder

Voltage(V)	Power Consumption(pW)	Delay(fs)
0.5	1.46	750.56
0.6	2.16	776.24
0.7	2.99	662.74
0.8	3.95	700.24
0.9	5.06	753.88
1.0	6.30	952.63

Table 2 presents the power consumption (pW) and delay (fs) of the proposed precharge low DCSL MTJ full adder at various voltages, ranging from 0.5 V to 1.0 V. It can be observed that both power consumption and delay increase as the voltage increases.



[Fig.8: Graph Showing the Power Consumption(pW) and Delay(fs) of Proposed Precharge low MTJ Full Adder at Different Voltages (V)]

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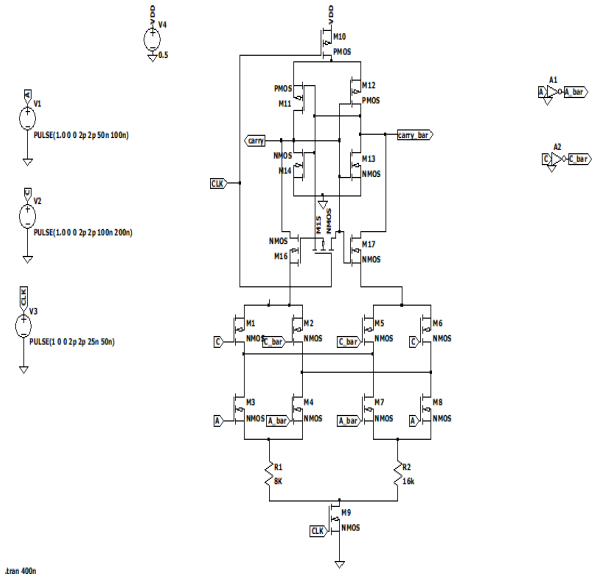
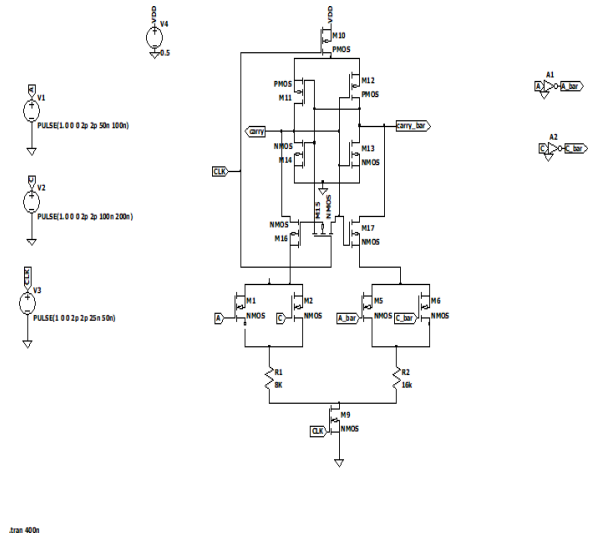
E. Proposed Improved Precharge Low DCSL MTJ Full Adder

The proposed precharge low DCSL full adder is improved, offering better delay and power consumption.



[Fig.9: The Design of Proposed Improved Precharge Low DCSL Whole Adder Sum Circuit in LTspice]



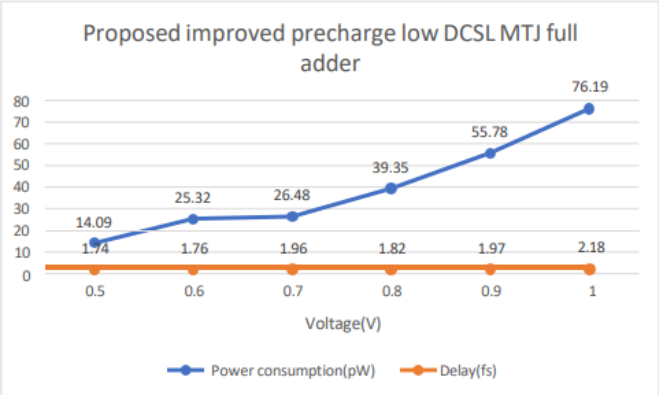
[Fig.10: The Design of Proposed Improved Precharge Low DCSL Full Adder Carry Circuit in LTspice]

F. The Output of the Proposed Improved Precharge Low DCSL MTJ Full Adder

Table III: Shows the Power Consumption and Delay of the Proposed Enhanced Precharge Low DCSL MTJ Full Adder]

Voltage(V)	Power Consumption(pW)	Delay(fs)
0.5	14.09	1.74
0.6	25.32	1.76
0.7	26.48	1.96
0.8	39.35	1.82
0.9	55.78	1.97
1.0	76.19	2.18

Table 3 presents the power consumption (pW) and delay (fs) of the proposed improved precharged low DCSL MTJ full adder at various voltages, ranging from 0.5 V to 1.0 V. As observed, the power consumption increases with increasing voltage. In contrast, the delay remains constant with minimal changes [15].



[Fig.11: Graph Showing the Power Consumption(pW) and Delay(fs) of Proposed Improved Precharge Low MTJ Full Adder at Different Voltages (V)]

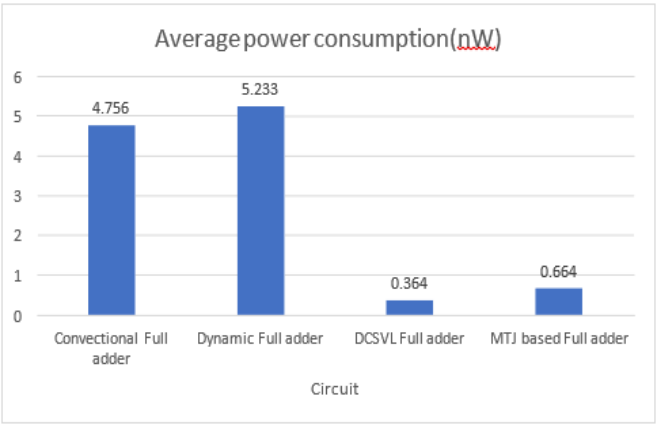
G. Comparison of Average Power Consumption and Average Delay of Full Adders

Thus, the different designs of full adders are implemented in LTspice software, and the power consumption and delay are measured at various voltages.

Table IV: Showing the Average Power Consumption (nW) and Delay(ps) for Different Circuits (Full Adders)

Circuit	Average Power Consumption(nW)	Average Delay(ps)
Conventional Full adder	4.756	5.17
Dynamic Full Adder	5.233	0.44
DCSVL Full adder	0.364	30.05
MTJ-based Full adder	0.664	1.99

Table 4 shows that the average power consumption (nW) is high for the dynamic full adder and low for the DCSVL full adder, whereas the delay (ps) is high for the DCSVL full adder and low for the dynamic full adder.



[Fig.12: Average Power Consumption(nW) of Different full Adders]

In Figure 12, one can observe that the dynamic full has a maximum power consumption (nW) of 5.233nW, and the DCSVL full adder has a minimum power consumption of 0.364nW.

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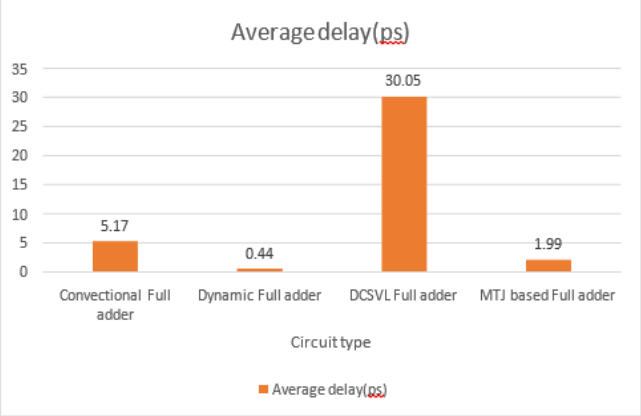
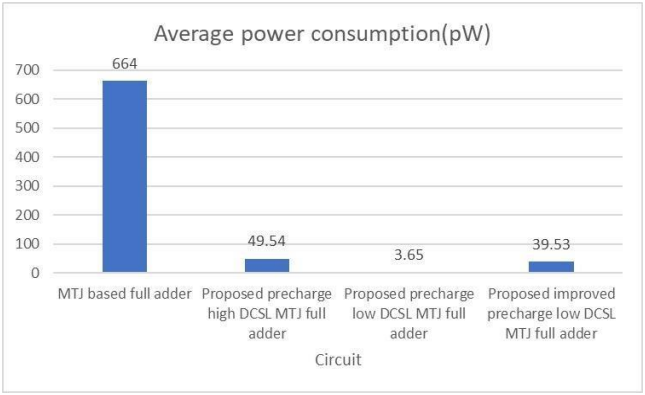


[Fig.13: Average Delay(ps) of Different Full Adders]

Figure 13 shows that the DCSVL full adder has a maximum delay (ps) of 30.05 ps, and the dynamic full adder has a minimum delay (ps) of 1.99 ps.

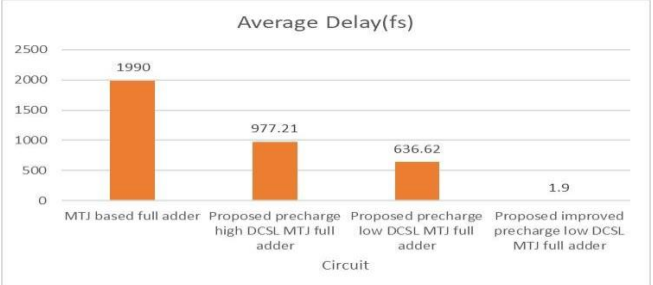
Table 5: Showing the Average Power Consumption(pW) and Delay(fs) for Different Proposed DCSL MTJ Full Adder Circuits

Circuit	Average Power Consumption(pW)	Average Delay(fs)
MTJ-based full adder	664.00	1990
Proposed precharge high DCSL MTJ full adder	49.54	977.21
Proposed precharge low MTJ DCSL full adder	3.65	636.62
Proposed improved precharge low DCSL MTJ full adder	39.53	1.90



[Fig.14: The Average Power Consumption of Proposed Precharge DCSL MTJ Full Adders]

Figure 14 shows that the MTJ-based full adder has high power consumption compared to the proposed precharge DCSL MTJ full adders. Among the proposed precharge circuits, the proposed precharge low DCSL MTJ full adder has minimum power consumption.



[Fig.15: The Average Power Consumption of Proposed Precharge DCSL MTJ Full Adders]

Figure 15 shows that the MTJ-based full adder has a high delay (fs), whereas the proposed improved Precharge low DCSL MTJ full adder exhibits a lower delay. We can infer from Figures 14 and 15 that the suggested enhanced precharge DCS low MTJ-based complete adder is more effective.

IV. CONCLUSION

The designs were simulated using the LTspice XVII software, and this work describes the design of the proposed precharged high DCSL MTJ full adder, proposed precharged low DCSL MTJ full adder, and proposed improved precharge low DCSL MTJ full adder. According to the results, the proposed precharge DCSL MTJ-based complete adder architecture consumes less power than other full adders. It also requires fewer transistors than other full adders. As a result, using the MTJ-based full adder to construct the non-volatile serial adder is a practical approach. These days, non-volatile serial adder circuits require a high supply voltage (V_{dd}), which is an energy-intensive operation. Scaling down V_{dd} is a valuable approach to reducing dynamic power consumption in low-power electronic devices, thereby satisfying the power budget. But lowering V_{dd} causes leakage power to increase. In the suggested system, we will have the whole adder circuit with the MTJ (Magnetic Tunnel Junction). We'll employ spin transfer torque (STT) MTJ circuits, which are used in most microprocessors and microcontrollers, and store binary bits (1 or 0) depending on the orientation and resistance that become parallel and anti-parallel.In the future, this project can be extended to build a Serial Adder using the MTJ-based full adder, as it is efficient and satisfies the required parameters.

DECLARATION STATEMENT

After aggregating input from all authors, I must verify the accuracy of the following information as the article's author.

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- **Ethical Approval and Consent to Participate:** The content of this article does not necessitate ethical approval or consent to participate with supporting documentation.
- **Data Access Statement and Material Availability:** The adequate resources of this article are publicly accessible.
- **Author's Contributions:** The authorship of this article is contributed equally to all participating individuals.

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