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Performance Evaluation of Different Topologies of SRAM and SRAM Memory Array Design at 180nm Technology

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Abstract: ***Memory circuits such as static random-access memory (SRAM) and dynamic random-access memory (DRAM) form an integral part of system design and contribute significantly to system-level power consumption. Memory operating speeds and power dissipation have become essential parameters due to the explosive growth of battery-operated appliances and the increased integration of circuits Hence SRAMs with different topologies are examined in terms of parameters like propagation delay, Static Noise Margin (SNM), corner analysis, and static power dissipation by simulating using versatile tool cadence virtuoso at 180nm technology. Besides, a topological performance comparison has also been illustrated, ranging from 2x2 to 8x8, thereby verifying the read and write modes of operation of SRAM.***

Keywords**: Corner** ***Analysis, Propagation Delay, SNM, SRAM Memory Array, Static Power Dissipation.***

I. INTRODUCTION

One of the most critical factors used to assess a device's performance is random access memory (RAM). Applications may temporarily store data and access it thanks to RAM. To facilitate rapid access, it stores the data that the device is currently consuming. Static Random Access Memory is a type of volatile memory that is powered on and off to maintain its value. Each data bit is stored using a bi-stable flip-flop circuit, a circuit commonly employed in computer cache memory. The main contribution of the paper is as follows:

1. To provide a direct interface with the CPU at speeds not attainable by DRAMs.
2. In systems that require very low power consumption.
3. SRAM plays a crucial role in memory storage due to its speed and energy efficiency.

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The primary considerations in CMOS VLSI design are time, power, and space consumption while constructing a circuit. The SRAM chip in gadgets satisfies these needs. Cell phones, wearables, and other consumer gadgets frequently employ SRAM chips. They are also incorporated into medical items, which can range from body area networks that contain several devices implanted in the body to hearing aids.

The flow of the work can be summarised in Section 1, which includes the introduction and organisation of the flow. Section 2 presents the schematics of various SRAM topologies simulated in Cadence using 180nm technology. Section 3 gives an insight into the modes of operation in SRAM. Section 4 provides an overview of the system used in implementing the SRAM memory array, which includes a decoder, multiplexer, sense amplifier, and various SRAM memory arrays, such as 2x2, 4x4, and 8x8. Section 5 signifies the performance evaluation and comparative analysis of different SRAM topologies. Section 6 draws significant conclusions from the work and the reference section.

II. DIFFERENT TOPOLOGIES OF SRAM

The different topologies of SRAM, 6T, 7T,8T, and 9T are constructed concerning [8], in order to compare the performance analysis and thereby choose the best and quicker SRAM topology to design the nxn SRAM memory array. The schematics of the various SRAM topologies (6T, 7T, 8T, and 9T) that are simulated by the Cadence Virtuoso tool are depicted in Figs. 1 to 4, respectively, at 180nm technology, as designed in [6], with a supply voltage of 2V is given to each topology of SRAM.

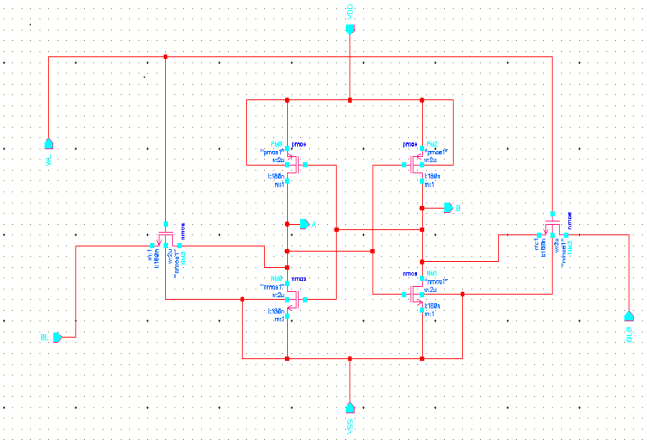

Fig. 1. Schematic of 6T SRAM

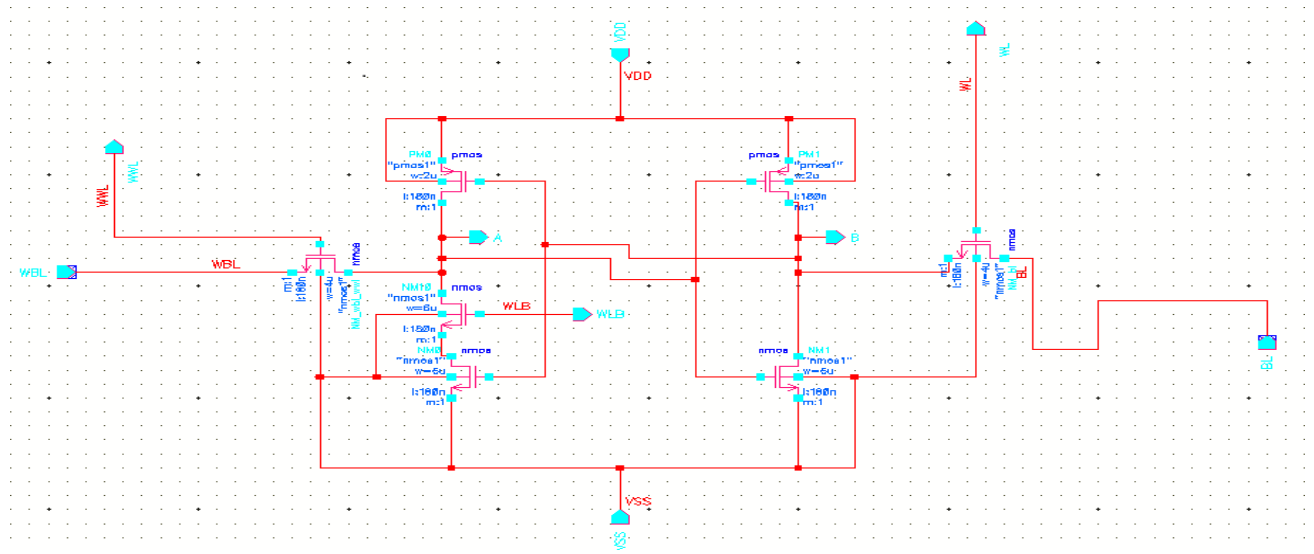

Fig. 2. Schematic of 7T SRAM

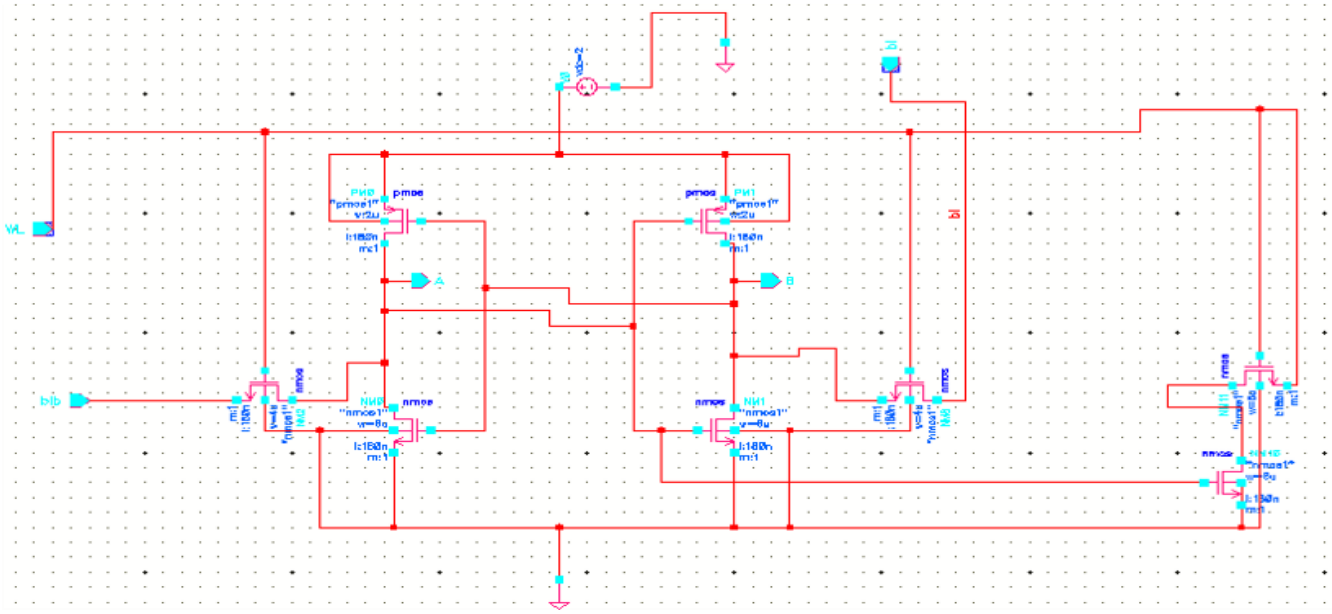

Fig. 3. Schematic of 8T SRAM

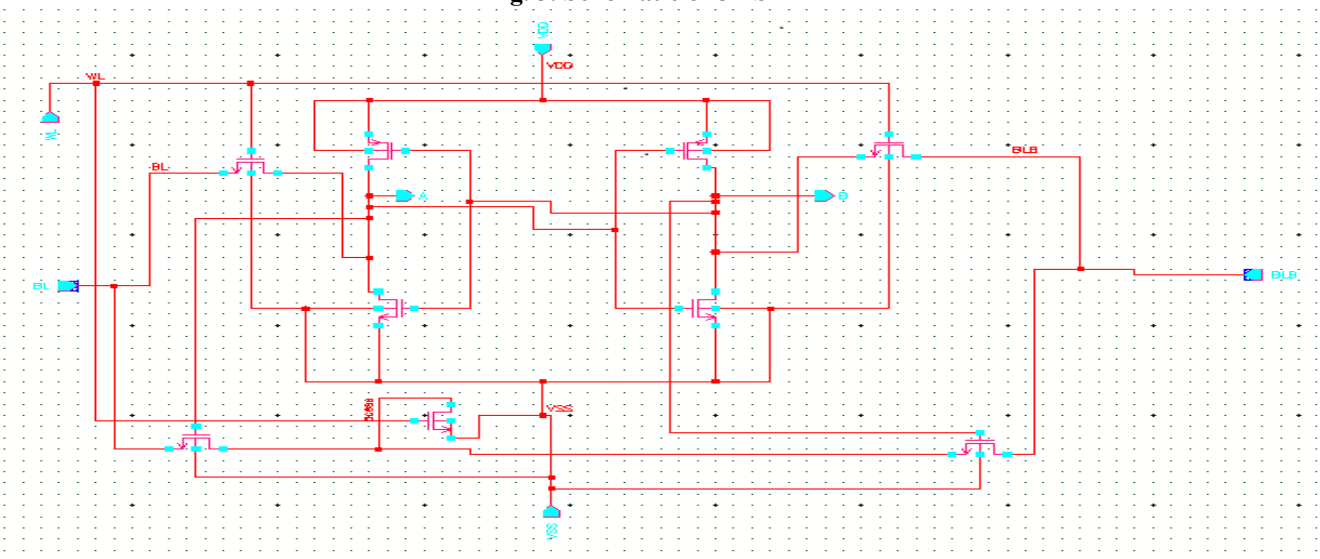

Fig. 4. Schematic of 9T SRAM

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III. DIFFERENT MODES OF OPERATION

SRAM functioning can be observed in three modes: hold, write, and read operations. The hold mode occurs when the SRAM's access transistors are in the off state, and no change in functionality is noticed; it is similar to a rest phase between read and write modes of operation. For different topologies of SRAM, here the simulation has been conducted to see read and write operations only [4].

The following stages can be used to demonstrate the read/write operations of the SRAM topology [7]:

Step 1: The Word line (WL)-connected access transistors are first switched ON. This starts the SRAM cell's read-and-write operations.

Step 2: Both bit lines are linked to the sensing amplifier during the read operation, which determines whether logic data "1" or "0" is recorded in the chosen memory address. The multiplexer then reflects the logic state at the output after receiving it from the sensing amplifier.

Step 3: Data from the input is sent to the write circuitry during the write operation. The data will be written to the SRAM since the write circuitry's drivers are more powerful than the cell's flip-flop transistors.

Step 4: The word line (row) is set to 0 V when the read/write operation is complete, making the system ready for the upcoming operation.

Individual SRAM topologies are simulated for read and write operations, where the output is fetched in the same manner as shown in Figs. 5 and 6, respectively.

The output of the 4x4 7T SRAM memory array in write mode is shown in Fig. 5. The first row and first column memory locations are enabled, as indicated by the markers in Fig.5, and data bits are written into that specific location of the memory array. The output of a 4x4 7T SRAM memory array in reading mode is shown in Fig.6. The first row and first column of the memory array are enabled, as indicated by the markers in Fig.6, and the previously stored written data bits from Fig. 5. are read and fetched output as stored.

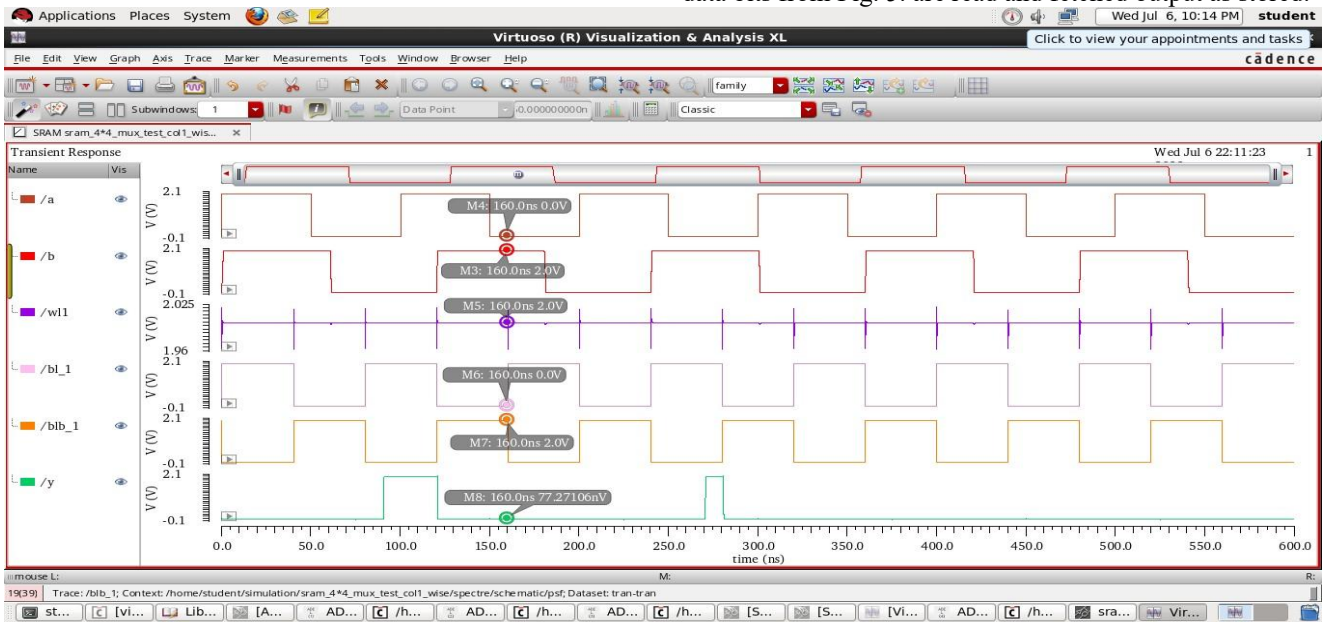

Fig. 5. Write mode output of a 4x4 7T SRAM memory array

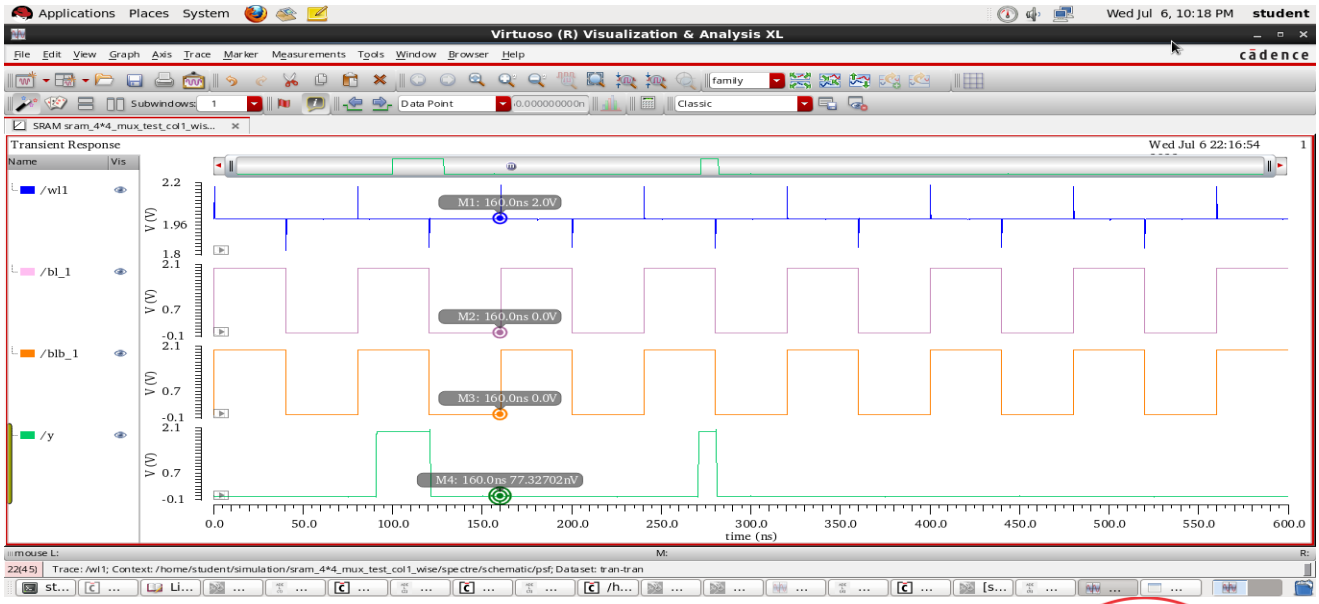

Fig. 6. Read mode output of 4x4 7T SRAM memory array

IV. SYSTEM OVERVIEW

Data is stored using a latch circuit in the volatile memory type known as static random-access memory (SRAM). Each SRAM cell stores one bit of data. Similar to DRAMs, RAMs can retain data without needing to be refreshed when power is applied, unlike DRAMs, which require periodic refreshes. All RAM memory blocks and topologies are implemented using the Cadence Virtuoso software. This intelligent system design environment utilises specialised IC technologies, including the Virtuoso platform, Spectre X, and AWR.

A. Block diagram of SRAM memory array

Fig. 7 depicts an SRAM memory array with n data inputs sent into the n:2n Decoder, which aids in activating one of the memory array's 2n word lines that serve as rows and the n-bit lines that act as columns. Each SRAM cell is coupled to one sense amplifier, and the nxn outputs of all memory array cells are sent into a 2n:1 multiplexer, which aids in mapping onto the designated memory address [11].

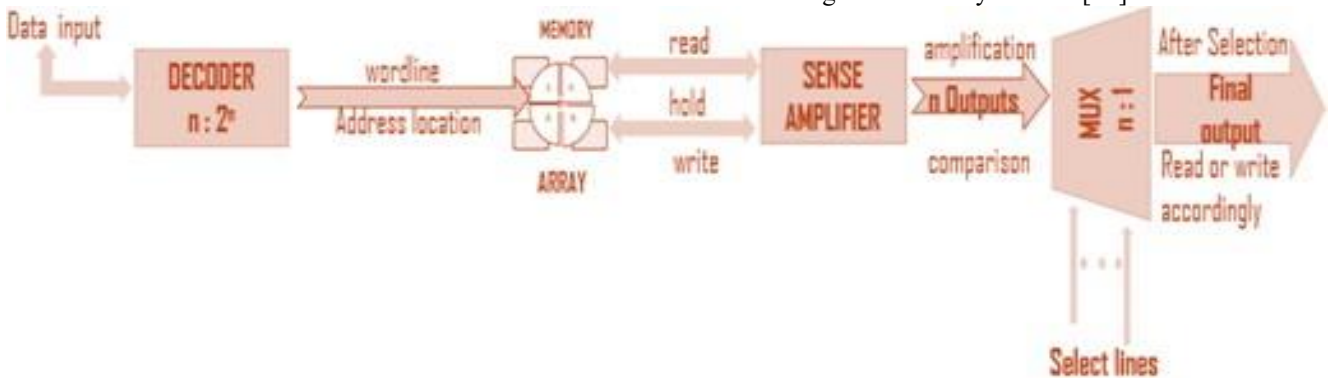

Fig. 7. Block diagram of nxn SRAM memory array

B. Decoder

Based on the binary row and column addresses, the decoder selects a specific memory location in the array. The word line in the memory array is selected using a combinational circuit. It contains a total of n input lines and 2^n output lines.

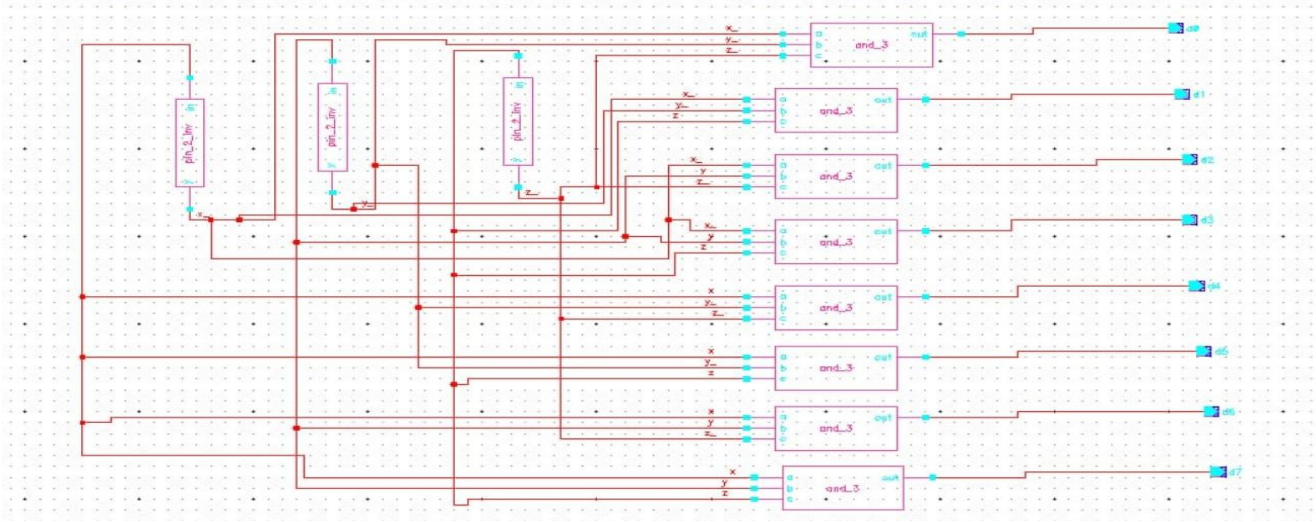

Fig. 8. Schematic of 3:8 Decoder

Depending upon the 2^n outputs of the decoder, the SRAM memory array size is fixed. For the nxn memory array, 2n number of outputs from the decoder serve as inputs. This helps power up one of the 2n word lines, which activates a particular row in the memory location. Fig. 8 is a 3:8 decoder that powers up one of the 8-word lines of the 8x8 SRAM memory array in Fig. 13, and thereby activating one of the eight rows of the memory array.

C. Memory array

The SRAM memory array is made up of SRAM cells organized in n rows and n columns, allowing for memory allocation for the storing of n bits [9]. A specific memory region in the array is mapped using word lines (rows) and bit lines (columns). The nxn SRAM cells include a sense amplifier, which detects the mode of operation of each cell and aids in signal amplification.

D. Sense amplifier

A sense amplifier is a component of the read circuitry that detects the voltage difference between the bit line and bit line bar to determine if a read or write operation is to be conducted and to amplify the output signal. Every cell has one sensory amplifier built in. Every SRAM cell's output is obtained from a sense amplifier. The multiplexer receives the outputs of the sensing amplifier as inputs in an n×n SRAM memory array.

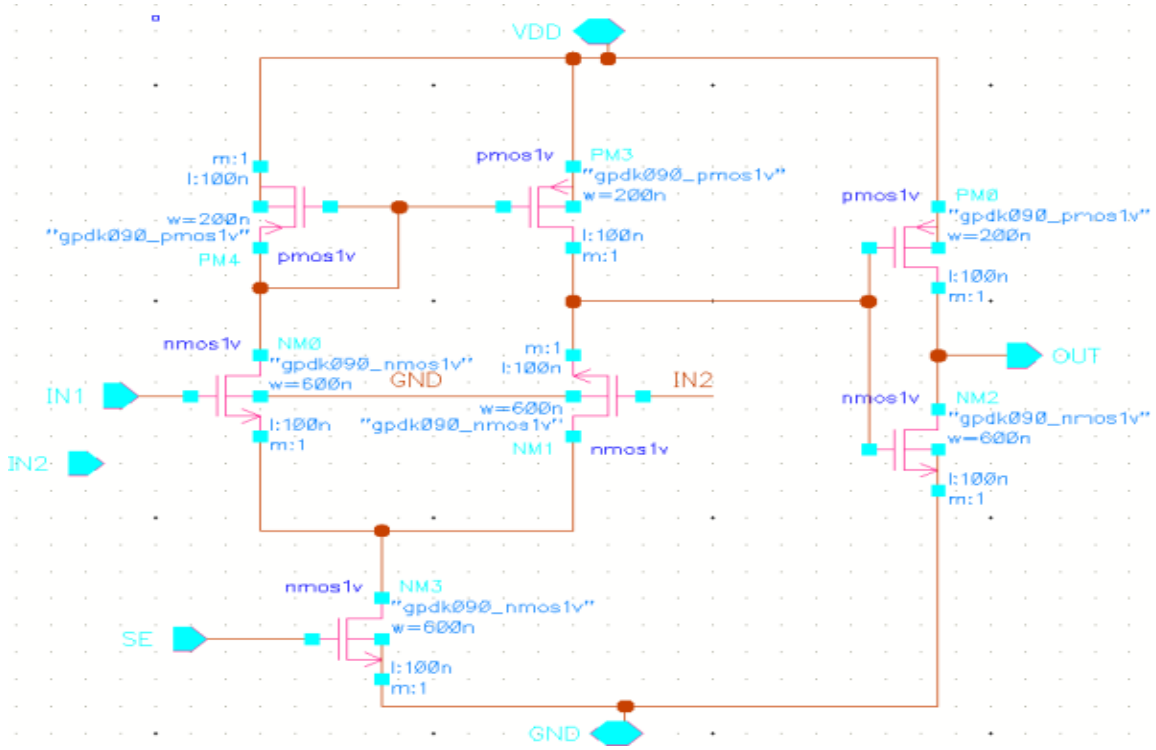

Fig. 9. Schematic of the Sense amplifier

The sensing amplifier is shown in Fig. 9. This is a crucial element in the design of a memory array. The sensing amplifier's job is to detect bit lines and bit line bars. As a result, memory cells read and write data more quickly and use less energy overall. The sensing amplifier's primary function during read/write operations is to magnify the voltage difference between the bit line and the bit line bar. It has several transistors that are involved in sensing, amplification, and memory function.

E. Multiplexer

A multiplexer has 2n inputs and one output. With the aid of select lines, it is possible to pick a specific cell from among the nxn SRAM cells in the array to read from it. The number of outputs from the SRAM cells determines which multiplexer to use. Fig.10. depicts a 4:1 multiplexer with two select lines. To read from a specific memory region of the 4x4 SRAM memory array, as shown in Fig. 12, the SRAM output is detected, amplified by the sense amplifier, and sent to the multiplexer to obtain the final output.

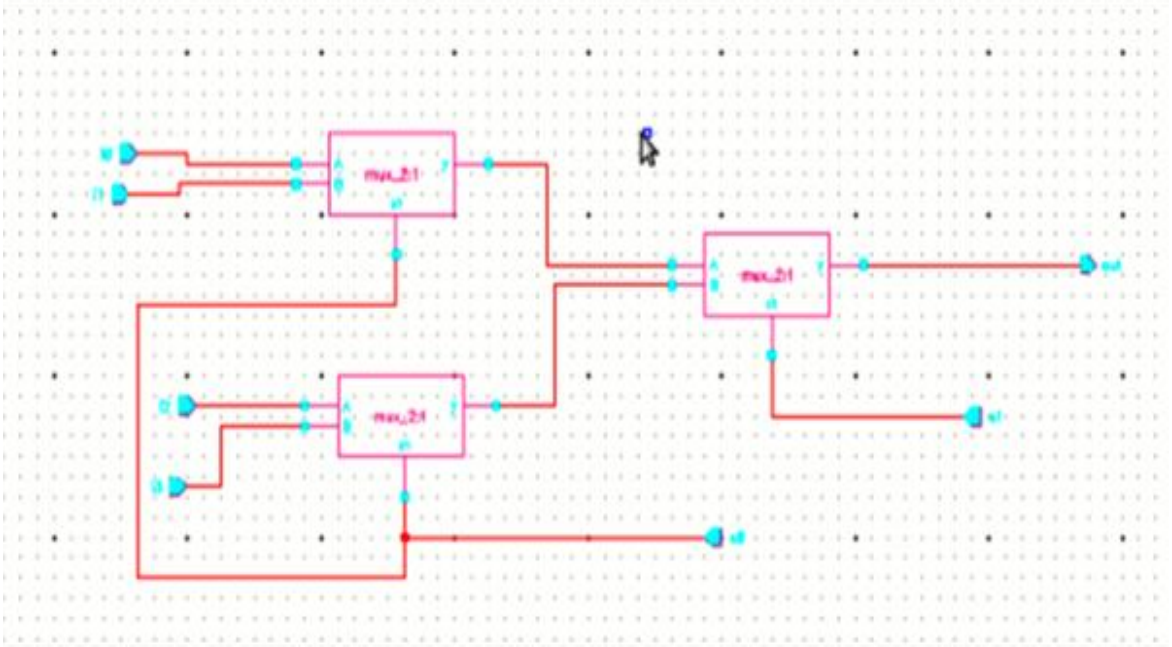

Fig. 10. Schematic of 4:1 multiplexer

V. SRAM NXN MEMORY ARRAY

The primary memory processing block is the nxn SRAM memory array, which consists of nxn SRAM cells. The SRAM cells may be of any of the topologies, such as 6T, 7T, 8T, or 9T, depending on the requirements. Each of these topologies is coupled to a Sense amplifier. The decoder's output word lines serve as rows, and bit lines serve as columns in the memory array.

For nxn memory array circuit optimization and to reduce glitches due to numerous wire connective shorts during the connection of circuits, the memory array has been constructed from a 2x2 size, followed by a 4x4 and then an 8x8 array of SRAM cells [11]. In all the cases of memory array connections, the word lines and bit lines are interconnected row-wise and column-wise, respectively.

A. SRAM 2x2 memory array

The 2x2 memory array shown in Fig. 11 has one data input going to the 1:2 decoder. The decoder's output serves as SRAM word lines, assisting in the activation of the memory's rows. The 4:1 multiplexer receives the 4 outputs from each cell of the SRAM array. When a read operation is to be performed, the multiplexer assists in selecting the specific memory region using two select lines.

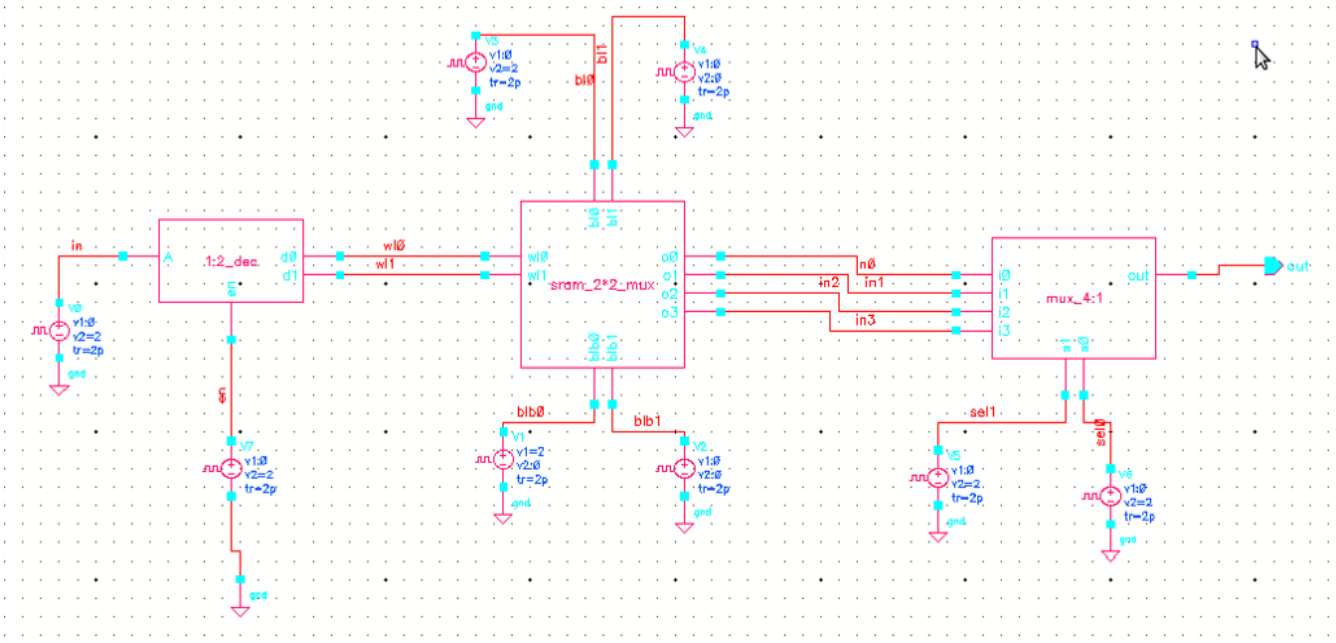

Fig. 11. Schematic of 2x2 7T SRAM memory array

B. SRAM 4x4 memory array

The 4x4 memory array shown in Fig.12 has a 16:1 multiplexer as its input device and a 2:4 decoder serving as its data input device. When a read operation needs to be performed, the multiplexer's four select lines help determine the specific memory location based on the specified row and column.

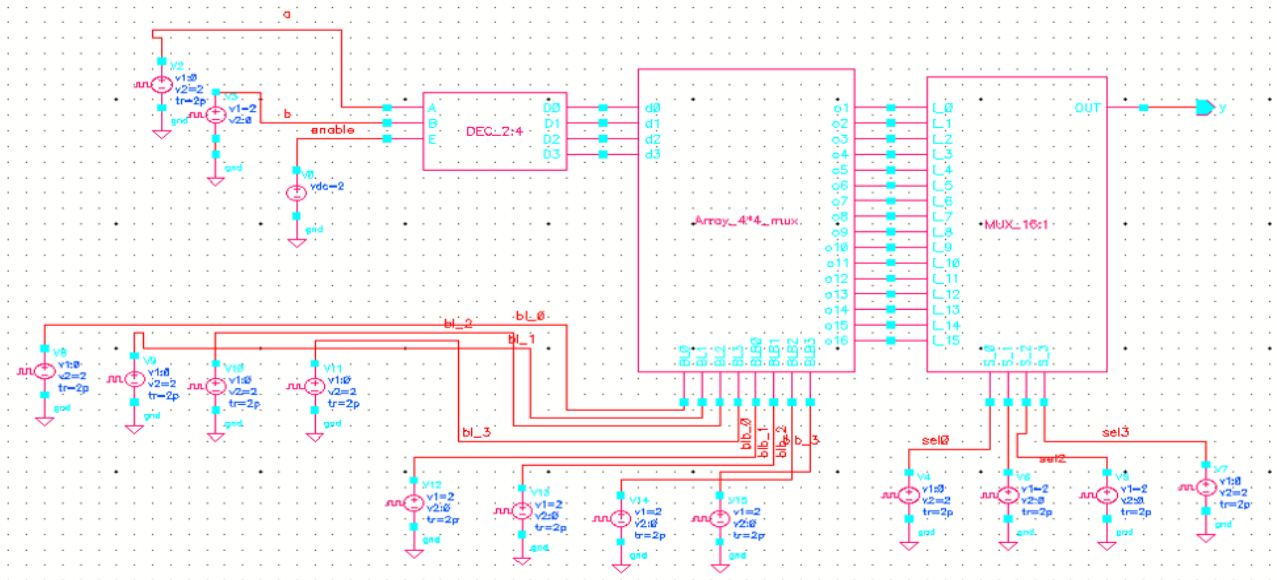

Fig. 12. Schematic of 4x4 7T SRAM memory array

C. SRAM 8X8 memory array

The 8x8 memory array [15] shown in Fig.13, requires a 3:8 decoder as its data input and 64 outputs from its SRAM array as input to its 64:1 multiplexer, which can be experimented with from a research point of view. When a read operation needs to be performed, the multiplexer's eight select lines help determine the specific memory location to access.

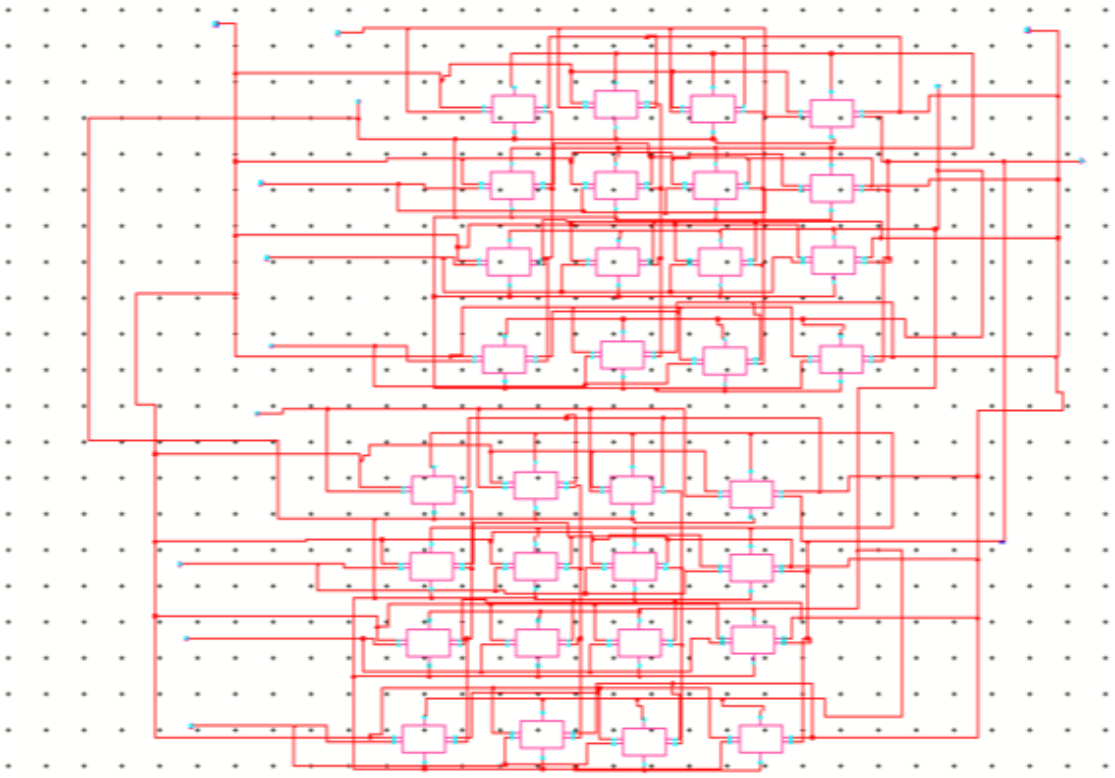

Fig. 13. Schematic of 8x8 7T SRAM memory array

SRAM topology	Read mode		Write mode		Propagation delay	
	Rise time (pS)	*Fall time (pS)*	*Rise time (pS)*	Fall time (pS)	Read mode (pS)	Write mode (pS)
6T	78.02	92.96	37.17	27.33	85.49	32.25
7T	52.05	44.55	36.79	27.33	48.30	32.06
8T	78.06	92.93	36.79	27.33	85.49	32.06
9T	78.03	92.95	37.02	29.33	85.49	32.17

VI. PERFORMANCE EVALUATION AND COMPARISON ANALYSIS

Speed, power, and area are the criteria that need to be optimized in the VLSI domain at each stage of design [14]. During read and writing operations, the different topologies of SRAM (6T, 7T, 8T & 9T) are examined with varying parameters of performance like propagation delay [7],[8], static power dissipation, static noise margin, and corner analysis.

A. Propagation delay

Propagation delay is the interval between when a logic gate's input becomes stable and valid and when the output of that logic gate becomes stable and valid.

Table- I: Propagation delay comparison

According to Table I, the 7T has a shorter propagation latency, which allows it to work more quickly by fetching the outputs earlier.

B. Static power dissipation

Designing an efficient SRAM that can operate at a higher speed with minimal energy loss requires careful consideration of its power usage [3],[5]. When the system is unpowered or at rest, leakage current—a form of static power dissipation—occurs. In other words, the power will be lost regardless of the system's switching and frequency [1]. In lower technology nodes, electrical leakage caused by leakage current continually and overwhelmingly predominates.

Table II: Static power dissipation comparison

SRAM topology	Static power dissipation	
	Read mode	Write mode
6T	1.343 mW	3.582 µW
7T	807.3 µW	2.434 µW
8T	1.343 mW	1.071 mW
9T	1.340 mW	3.396 µW

Table II tabulates the static power dissipation of different topologies of SRAM (6T, 7T, 8T, 9T) [6] which can be calculated by averaging the leakage current obtained in each case of the SRAM topologies [2] with the help of the Cadence calculator. Among all the topologies, 7T is faster during both read and write operations with less static power dissipation.

C.Static Noise Margin (SNM)

Integrated circuits are more susceptible to noise at low levels because they must fit into smaller spaces [12], which causes supply lines and other sources to generate noise signals. The circuit becomes less stable and less effective as a result. The finest illustration of an integrated circuit is SRAM. SRAM is primarily used in portable electronics and high-performance circuits where energy-efficient memory is required. Therefore, maintaining a properly working circuit in the presence of a noise source is crucial.

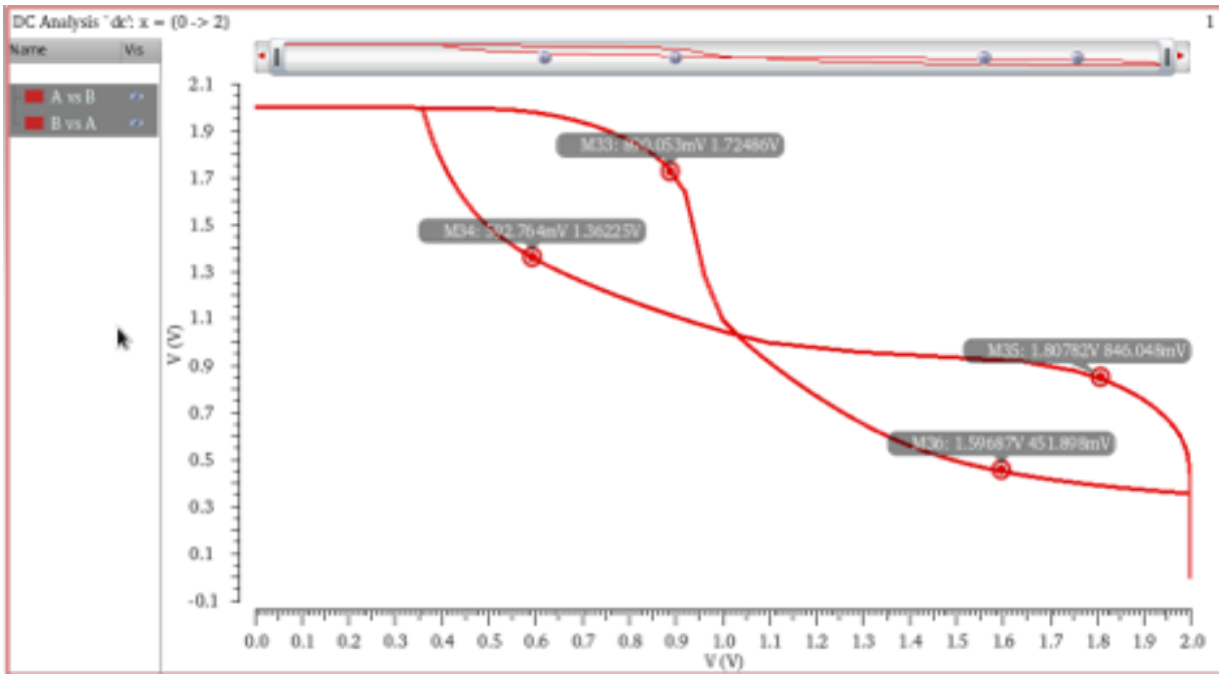

Fig. 14. Butterfly plot of 7T SRAM to obtain SNM

Fig.14. displays the SRAM cell's butterfly plot, which is used to determine the Static Noise Margin (SNM). The value of SNM is determined by the Euclidean distance between the diagonal ends of the butterfly plot's biggest square [13]. The comparison of SNM for all topologies is tabulated in Table III Comparatively, the SRAM 7T has the greatest SNM.

Table III: Static Noise Margin (SNM) comparison

SRAM Topology	Write Mode (V)	Read Mode (V)
6T	0.4633	0.726
7T	1.0901	0.9973
8T	0.9662	0.9147
9T	0.4998	0.7682

D.Corner analysis

Any integrated circuit that is to be manufactured must first undergo several pre-processing steps, including UV exposure, photoresist coating, and ion implantation, among others. The operating voltages and temperatures for these various operations will vary. Corner analysis must be done in line with Process, Voltage, and Temperature (PVT) to ensure that the SRAM is made to endure such harsh circumstances [10]. The resilience of the circuit will be ensured by modelling the intended circuit at various process, voltage, and temperature corners.

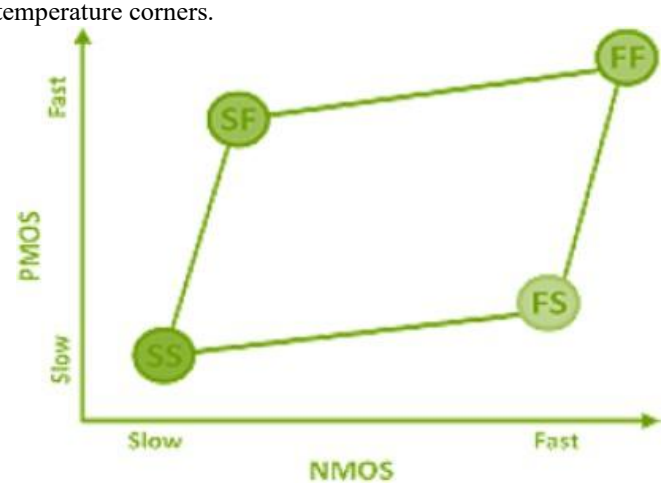

Fig. 15. Corners mapping plot

The corners as shown in the plot in Fig. 15 are Slow NMOS Slow PMOS (SS), Slow NMOS Fast PMOS (SF), Fast NMOS Slow PMOS (FS), and Fast NMOS Slow PMOS (FF).

Table IV: Corner analysis comparison

Process Corner	6T		7T		8T		9T	
	Write mode	Read mode	Write mode	Read mode	Write mode	Read mode	Write mode	Read mode
SF	1.651mS	2.97 nS	1.661 mS	3.02 mS	1.670 mS	3.12 mS	1.680 mS	3.19 mS
FS	417.8 pS	32.64 nS	421.2 pS	32.69 pS	423.3 pS	32.12 nS	425.4 pS	32.84 nS
SS	559.9 pS	1.739 nS	560.2 pS	1.760 nS	562.3 pS	1.769 nS	563.4 pS	1.771 nS
FF	1.241 nS	45.51 nS	1.267 nS	45.87 nS	1.281 nS	46.02 nS	1.301 nS	46.21 nS

According to Table 4, with respect to read and write operations, 6T, 7T, 8T, and 9T SRAM cells write more quickly at the SS corner. The quickest of them is found to be 9T SRAM.

VII. RESULT AND DISCUSSION

The different topologies of SRAM (6T, 7T, 8T, and 9T) are compared in terms of performance evaluation. The SRAM memory array is illustrated, progressing from a primary 2x2 to an 8x8 array. In search of a better-featured SRAM topology, various performance parameters are considered, including propagation delay, Static noise margin (SNM), corner analysis, and static power dissipation. These parameters are used to simulate each SRAM topology using the Cadence Virtuoso tool. Among the simulated topologies of SRAM, 7T was found to be an efficient one with a propagation delay during read and write modes are 48.30pS and 32.06pS respectively, Static noise margin (SNM) of 1.0901V and 0.9973V during write and read modes respectively, the static power dissipation of 807.3 µW and 2.434 µW during write and read modes of operation. With the corner analysis approach, all SRAM topologies are faster at the SS corner.

VIII. CONCLUSION

The different topologies of SRAM (6T, 7T, 8T, 9T) are simulated using the Cadence Virtuoso ADE tool at a 180nm technology node. A comparison of performance analysis in terms of propagation delay, Static noise margin (SNM), corner analysis, and static power dissipation has been done. Additionally, SRAM memory arrays (2x2, 4x4) are also verified to ensure proper read and write operations. The ARAM memory array may be constructed using any one of the SRAM topologies (6T, 7T, 8T, 9T). Here, after inquiring about the best performance in terms of the specified parameter, 7T SRAM is found to be quicker in operation. The 7T SRAM 4x4 memory array is successfully simulated, allowing it to read and write data to the available memory locations.

FUTURE SCOPE

This work can be further extended to simulate a high-end 10T device based on an SRAM memory array, which exhibits improved characteristics in terms of stability and performance. The 8x8 SRAM memory array can also be examined in terms of its reading and writing modes of validation, for which a 64:1 multiplexer needs to be designed from our perspective. This is a bit challenging and requires replacement by some other selection criteria. All the SRAM topologies were simulated at 180nm technology using the Cadence tool, which can also be experimented with in 90nm, 45nm, or any other optimised technology. Effort delay can be taken into further consideration to gather information about the PMOS and NMOS width variations that need to be implemented to achieve the best results. Power reduction techniques can be implemented using the sleep approach, as well as the adiabatic and stack techniques, which are best known for their energy efficiency.

DECLARATION

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Ethical Approval and Consent to Participate	No, the article does not require ethical approval or consent to participate, as it presents evidence that is not subject to interpretation.
Availability of Data and Material/ Data Access Statement	Not relevant.
Authors Contributions	All authors have equal participation in this article. Authors are required to include a declaration of accountability in the article, including review-type articles, that stipulates the involvement of each author. The level of detail differs; some subjects yield articles that consist of isolated efforts that can be easily detailed, while other areas function as group efforts at all stages.

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