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Performance Evaluation of Approximate Adders: Case Study

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Abstract*: A computing device designed to carry out a variety of arithmetic computations. The adder circuit, whose operation must be quick with a small area of occupancy, performs the addition, which is a necessary operation in many other mathematical operations including subtraction, multiplication, and division. There is a mandate for an adder circuit with minimal power consumption, minimal delay, and minimal size in various real-time applications such as processing of signals, pictures & video, VLSI data pathways, processors, neural networks, and many more. There is a new class of adders called approximation adders that operate inaccurately but with favorable area, speed, and power consumption. Since their output is inaccurate, the other names for approximate adders are imprecise adders. This set of adders operates at a high speed thanks to a circuit critical path design that uses fewer components. Additionally, compared to precise adders, the approximate adder circuit has a relatively low component count, resulting in a small footprint and circuits that use less energy. There are different ways to create approximate adders. The area can be predicted by counting the number of circuit components that are present. By examining a number of the critical path's components, delay can be predicted. Several errors that appear in the output of the particular circuit can be used to calculate the accuracy percentage. This review compares approximate adders from four different categories across the board in terms of design constraints and makes note of the differences between each adder.

***Keywords*: Approximate Adder, Approximate Mirror Adder (AMA), Approximate Adders using XOR/XNOR gates (AXA), Accuracy, Approximate Adder Designs (APAD).**

I. INTRODUCTION

This Because it performs fundamental arithmetic operations including addition, subtraction, and multiplication [1], [2], [3], [4], an adder is a crucial component in every computer system. A half adder's primary idea is to add two bits without carrying them, whereas a full adder adds three bits—two input bits plus one carry input bit—instead. There are numerous adder topologies that fall into various categories, including Ripple Carry Adders (RCA), Carry Look-Ahead Adders (CLA), carry skip adders (CSA), and Carry Select Adders (CSLA) [5], [6] and [20]. These conventional adders have problems with them. The fundamental idea of Carry generation and propagation functions inherent in CLA [7, [8] is used in the design of a set of adders known as Parallel propagation adders (PPAs). The fundamental benefit of PPAs is their high-speed operation, but because of their complexity, they have larger circuit areas and consume more power. However, a contemporary and effective VLSI circuit must meet three requirements: small size, low power consumption, and fast speed [9].

A group of adders known as approximation adders have been presented [10] to get around this need of VLSI circuit design specifications. The degree of precision in the outcome and the design limitations distinguish accurate from approximate adders. The outcome of an accurate adder is an exact value, but its design limitations - such as size, speed, and power consumption - are inadequate. For some input bit combinations, the sum and carry output result in approximate adders is inaccurate, but its area, speed, and power consumption design limitations are greatly tightened [11].

There is a need to create unique designs for approximate arithmetic since approximate computing circuits like adders and multipliers [12], [13], and [14] are becoming more and more prevalent. The ability to create circuits with better performance increases with the freedom from mathematically correct conclusions. Although the outputs of the approximate circuit are not mathematically accurate for all combinations of inputs, its performance is improved [15], [16], [17]. Applications for processing images and videos are error-tolerant, allowing for a large increase in processing speed and a reduction in power consumption at the expense of quality. The level of operation precision varies depending on the application. Circuits with varying degrees of precision are occasionally needed for applications that are comparable, and these requirements can alter over time. Since addition is a fundamental part of arithmetic computation, greater attention must be paid to approximate adder design. Reduced power consumption in the circuit is essential for developing an approximate adder with an approximate output because the adder section uses more power on the die [18]. This paper mainly discusses various approximate adder types, outlining the advantages and disadvantages of each. The remainder of the essay is partitioned into two segments.

Section 2 provides a quick summary of the literature on approximate adders. Section 3 describes how various approximate adders function with its speed which is elaborated in Section 4, which uses speed as a measure of a circuit's performance.

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In Section 5, the many applications of these adders are briefly described. The paper winded up with conclusion and a future scope.

II. LITERATURE SURVEY

Most processors and data channels require circuits with little power consumption, minimal space, and minimal delay. An adder block in any circuit uses more power than the rest of the chip, as was mentioned in the preceding section. This results from the propagation delay of the carry bit from the LSB bit to the MSB bit. The adder block's power consumption will increase if the propagation path is long. The carry propagation path must be brief in order to meet the requirements of least area, highest speed, and least power consumption. Some of the frequently discussed adder topologies include the RCA, which is simple to construct and use but has a long carry propagation path that adds to the circuit's delay. The propagation path for the CSA, CSLA, and CLA circuits is short, but their structure and operation are complex. There have been many lower power dissipation adders proposed [22], but the delay is greater. Approximate adder circuits are created at the expense of output precision to solve the delay and power issues. Error Tolerant Adders (ETA) or imprecise Adders are other names for approximate adders. Ning Zhu et al. create an ETA [23] in 2010 that works by separating the input bits into accurate and imprecise sections. The 2013 design by Vaibhav G, et al. changed the mirror adder [6] into five distinct approximate mirror adder (AMA) [24] circuits. By lowering the number of transistors in the mirror adder circuit's internal circuit design, AMAs are created. Approximate XOR/XNOR based adders (AXA) were developed by Zhixi. Y. et al. in 2013 [25]. Y. Kim, Y. Zhang, and P. Li in 2015 introduced an approximation adder with lower power consumption and a very low fault rate [26] that is used for neuromorphic computing. Z. Yang et al. created an approximate adder employing transmission gates in 2015 [27] for low-power applications. Irina Alam and KT Lau proposed an inaccurate adder circuit with low-power intake and delay in 2016[28]. Truncated power logic applications use the Carbon Nanotube Field-Effect Transistor (CNFET). Atiyeh Panahi et al. suggested two roughly CNFET-based ternary adders in 2016[29] using this technology. A unique approximate adder structure was created in 2017 by Junjun Hu and colleagues to address the issue of output quality degradation brought on by erroneous results in approximate adders [30]. In order to give a methodical approach for constructing approximate adders, Ardalan Najaf et al. suggested a hybrid approximate adder strategy in 2018 [31]. Ayad Dalloo et al. created an optimised Lower Part Constant-OR Adder (LOCA) in 2018 to demonstrate development together error and circuit cost measures. With the aid of a fake timing path notion, Vincent Camus and Jeremy Schlachter created a new approximate adder in 2018 [32] known as the carry cut back adder. A carry prediction-using accuracy configurable adder (ACA) is created using the approximation approach. Wenbin Xu et al. suggested the ACA in 2018[33]. High-Performance Error Tolerant Adders (HPETA), which have a multiplexer-based strategy, were proposed by R. Jothin and C. Vasanthanayaki in 2018 [34]. Sunil Dutt et al. suggested the Equal Segment Based Approximate Adder (ESAA) in 2018 to improve accuracy, latency, and power [35]. Additionally, ESAA makes use of logic for mistake detection and correction [7]. Soares et al. created a novel hybrid approximation adder in 2019 employing PPAs for accelerator architectures [36].
Sunil Dutt et al. created an improved ESAA in 2019 that has an ideal configuration, a minimal amount of delay, and an area that can be exploited to increase accuracy [37]. Li Luo et al. introduced a Single Clock Cycle Approximate adder (SCCA) in 2019, which reduces overall circuit delay and executes addition operation in a single clock period [38]. Ebrahimi - Azandaryani et al. recommend a Block based Carry Speculative Approximate Adder (BCSA) architecture in 2020 that uses less power and suffers from reduced accuracy loss [39]. A system for mistake identification and recovery is also present in BCSA. G. Anusha and P. Deepa in 2020 suggested seven types of approximate adders for error-tolerant image processing with decreased time and power consumption [40]. Nojehdeh ME and Altun M. have proposed four new types of adder designs (APAD) in 2020 that require less space and use less power [41].

III. CATEGORIES OF APPROXIMATE ADDERS

The literature evidencing that the approximate adders are proposed and analyzed in numerous ways like speculative adders, segmented or block-based adders, approximate full adders [42]. The adders in which the critical path is rarely triggered are called Speculative adders. Segmented adders are also called block-based adders in which the entire n-bit adder is alienated into various small blocks of adders. Finally, the approximate adder's category works on the approximation principle on sum and carry output. Approximate adders are single bit adders. In another way, approximate adders are simply classified into two types-1. Single bit adder block using which larger adder blocks are designed 2. Directly larger adder blocks are designed. Fig 1depicts in detailed approximate adder classification with example adder designs.In this section, Approximate full Adders will be discussed in detail which are designed by using Mirror Adders called AMA [24], approximations on sum and carry called AA [40], XOR/XNOR gates called AXA [33], and by the idea of using offsetting errors which are called Approximate adder design APAD [41]. All the adders discussed are single-bit input size.

A. Approximate Mirror adders (AMA)

The critical path of the mirror adder [6] circuit consists of a minimum no. of transistors. In the circuit also there is less delay and area when compared to a conventional full adder circuit. This circuit is modified further to circuits having decreased delay, area, and power dissipation. Five different AMA circuits are proposed in [24]. The sum and carry output [19] expressions for basic full adder (FA) and AMA circuits are given as:

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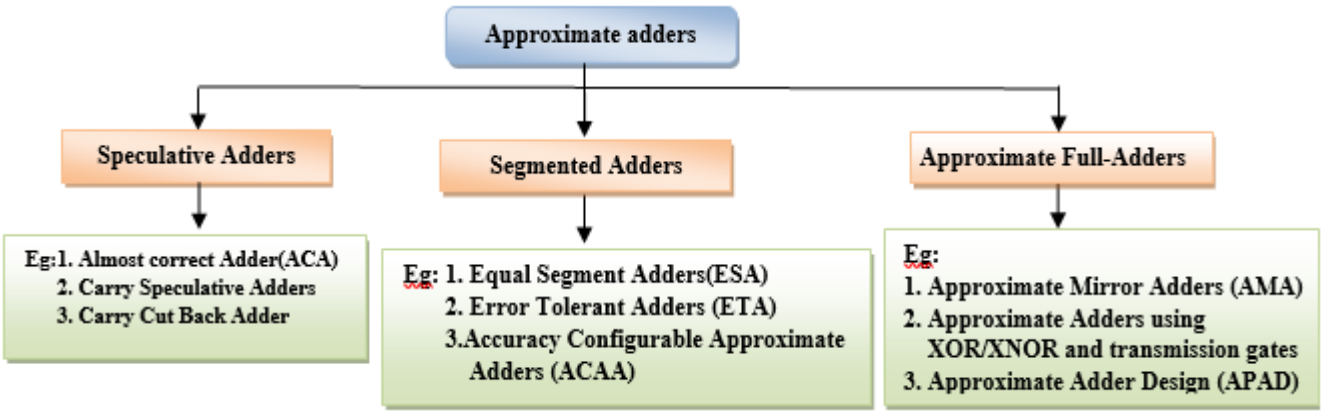

Fig. 1.Classification of Approximate Adders

Table-I. The Logic table for Full Adder, different AMAs, and AXAs (Note: Error denoted by X) [24], [25]

INPUTS			OUTPUTS																	
			FA		AMA1		AMA2		AMA3		AMA4		AMA5		AXA1		AXA2		AXA3	
A	*B*	*Cin*	*S*	*Cout*	*S*	*Cout*	*S*	*Cout*	*S*	*Cout*	*S*	*Cout*	*S*	*Cout*	*S*	*Cout*	*S*	*Cout*	*S*	*Cout*
0	0	0	0	0	0	0	1X	0	1X	0	0	0	0	0	0	0	1X	0	0	0
0	0	1	1	0	1	0	1	0	1	0	1	0	0X	0	1	0	1	0	1	0
0	1	0	1	0	0X	1X	1	0	0X	1X	0X	0	1	0	0X	1X	0X	0	0X	0
0	1	1	0	1	0	1	0	1	0	1	1X	0X	1X	0X	1X	0X	0	1	0	1
1	0	0	1	0	0X	0	1	0	1	0	0X	1X	0X	1X	0X	1X	0X	0	0X	0
1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	1X	0X	0	1	0	1
1	1	0	0	1	0	1	0	1	0	1	0	1	1X	1	0	1	1X	1	0	1
1	1	1	1	1	1	1	0X	1	0	1	1	1	1	1	1	1	1	1	1	1

i) For FA:

$$S = A \oplus B \oplus Cin \quad \& \quad Cout = AB + BCin + CinA \tag{1}$$

ii) AMA1:

$$S = ABCin + \overline{Cout}.Cin \ \& \ Cout = ACin + B \tag{2}$$

iii) AMA2:

$$S = \overline{Cout} \ \& \ Cout = AB + BCin + CinA \tag{3}$$

iv) AMA3:

$$S = \overline{Cout} \ \& \ Cout = ACin + B \tag{4}$$

v) AMA4:

$$S = ABCin + \overline{Cout}.Cin \ \& \ Cout = A \tag{5}$$

vi) AMA5:

$$S = B \ \& \ Cout = A \tag{6}$$

B. Approximate Adders using XOR/XNOR Gates (AXA)

These adders are designed using XOR/XNOR gates. In [25], three AXA circuits are proposed which are-1. AXA1 is proposed using the XOR gate in [43] 2. AXA2 and AXA3 are proposed using an XNOR gate having four transistors [44]. Table-I represents the full adder, AMA, and AXA which shows the errors occurring in different adders for different input combinations. The sum and carry output expressions for AXA circuits are as follows:

vii)AXA1:

$$S = Cin \ \& \ Cout = A\overline{Cin} + AB + B\overline{Cin} \tag{7}$$

viii)AXA2:

$$S = \overline{AB} + AB \quad \& \quad Cout = AB + BCin + CinA \tag{8}$$

vii) ix)AXA3:

$$S = \overline{AB}Cin + ABCin \ \& \ Cout = AB + BCin + CinA \tag{9}$$

C. Approximate Adders (AA) using an Approximation

These are designed by taking reference of AMAs and considering approximations in sum and carry output [40]. Seven different types of AAs are designed. Table 2 depicts the comparison between the full adder and anticipated approximate adders. The sum and carry output expressions for AA circuits are as follows:

i)AA1:

$$S = \overline{A} + BCin \quad \& \quad Cout = A \tag{10}$$

ii)AA2:

$$S = (\overline{A}(B + Cin) + BCin) \ \& \ Cout = AB + BCin + CinA \tag{11}$$

iii)AA3:

$$S = (\overline{A} + B)Cin \ \& \ Cout = AB + BCin + CinA \tag{12}$$

iv)AA4:

$$S = \overline{AB} + \overline{BCin} + ABCin + \overline{A}\overline{BCin} \ \& \ Cout = AB + BCin + CinA \tag{13}$$

v)AA5:

$$S = \overline{A} + BCin \quad \& \quad Cout = AB + BCin + CinA \tag{14}$$

vi)AA6:

$$S = \overline{A}(\overline{B} + \overline{Cin}) + \overline{A}B\overline{Cin} \ \& \ Cout = AB + BCin + CinA \tag{15}$$

vii)AA7:

$$S = AB + B\overline{Cin} + \overline{AB}Cin + A\overline{BCin} \;\&\; Cout = AB + BCin + CinA \quad (16)$$

D. Approximate Adder Designs (APAD)

These adders are designed using offsetting errors and choosing solutions having the minimum sum of product expressions [41]. Four different APAD designs are proposed whose truth table comparison with full-adder is shown in Table-III.

The sum and carry output expressions for APAD circuits are as follows:

i)APAD1:

$$S = ABCin + A\overline{BCin} + \overline{A}B\overline{Cin} \;\&\; Cout = B + ACin \quad (17)$$

ii)APAD2:

$$S = \overline{A}B + BCin + \overline{A}Cin \;\&\; Cout = A \quad (18)$$

iii)APAD3:

$$S = \overline{A}Cin + B \;\&\; Cout = A \quad (19)$$

iv)APAD4:

$$S = B \;\&\; Cout = A \quad (20)$$

IV. RESULT ANALYSIS

The operation of 19 approximate adders is analyzed in section 3. From the truth table of respective adders, their output expressions are obtained. From those expressions, one can obtain the CMOS technology-based circuit diagram of the respective adder. CMOS technology-based circuits have more advantages like low power consumption, high packing density, Bidirectional capability, and many more when compared to other technology circuits which is the foremost reason to choose CMOS-based circuit implementation. With the help of the circuit diagram, the area-expanse and speed of the respective adder can be calculated i.e. area can be calculated by the counting number of transistors that appear in the schematic. Also, with the help of transistor count present in a critical path, the delay can be calculated.

In CMOS circuits, two transistors (one PMOS and one NMOS) are required for each literal sum of product term present in the output equation of the track. Let us go with $S = (AB + \overline{Cout})Cin$ and $Cout = ACin + B$. The area calculations of discussed approximate adders are as follows: wrt no of transistors i.e. total no. of transistors required= (total no. of literals*2) + (total no. of inverters required *2). Ex: No. of literals in S and Cout equation=7; and No. of inverters required=1

Total no. of transistors required = (7*2) + (1*2) = 14+2=16

A full adder CMOS circuit consists of 28 transistors [6]. Also, from the truth table of respective adders, one can be able to calculate the accuracy depending upon the number of errors the circuit produces in both the outputs. E.g., consider the AMA1 adder which is having a total of 16 output conditions (8 sum output conditions and 8 carry output conditions) for 8 different input combinations. In 16 output conditions, the total number of errors that take place is 3. The percentage of accuracy for AMA1 is calculated as- Accuracy % for AMA1= [(total no. of outputs- no. of errors in output)/total no. of outputs] *100 = [(16-3)/16] *100=81.25%.

In a similar approach, the accuracy percentage for the remaining adders is calculated. All the discussed adders in section 3 are contrasted with each other on basis of area, delay, and accuracy. The expressions for sum and carry out of AMA5 and APAD4 are the same due to which only one design is taken for comparison. Table-5 spectacles the area, delay, and exactness parameters of all adders. As shown in table 5, the different AMA circuit's area and delay is less when compared to other category adders but accuracy is medium. The AMA5 area and delay are 0 but its accuracy is 62.5% which low. Among AMA circuits, AMA2 is having good accuracy with less delay and area. In different

AXA circuits, AXA1 is having less area and delay but its accuracy is very poor i.e., 50% whereas AXA2 and AXA3 have more area, less delay, and good accuracy. So, it can be said that in AXA circuits there is a tradeoff between area and accuracy i.e., as area decreasing accuracy is also decreasing.

The next category of adders is AA in which the accuracy level is good but the area is increased when compared to AMA circuits. Among AA circuits, AA5 is having an average area, less delay, and average accuracy of 81.25%. The last category of adders is APAD circuits in which the same phenomenon continues i.e., as the area decreases accuracy decreases. All three APAD circuits are having the same delay. In APAD circuits, APAD2 is considered to be better when compared to the other two circuits as it is having average area and accuracy. Fig 2 & 3 depicts the comparison graph basing parameters like area, accuracy, and delay among different adders. From the graphs, it can be said that as the area is decreasing the accuracy of the circuit is also decreasing. The same can be seen in Table 4 also that the circuits with high accuracy are having a high area.

V. APPLICATIONS

As discussed in previous sections the adder forms a major block in many circuits. There is a huge range of applications that can be implemented using the adders reviewed in this paper. Multipliers play a dynamic role in the design of many video, signal, and image processing units [9], [45]. When compared to other arithmetic [21] applications like addition and subtraction, multiplication consumes more time, and hardware implementing multiplication operation occupies more area. As addition plays a key role in multiplication operation, approximate adders can be used in the design of multiplier circuits. The main advantage of approximate adders is less delay and the low area which can be used to design a high-speed and area-efficient approximate circuits can be designed using these adders. Multipliers are divided as array multipliers and tree multipliers in which tree multipliers are faster in operation but occupy more area.

To overcome the problem of more area in tree multipliers, approximate tree multipliers can be designed using the approximate adders. An approximate Dadda multiplier(ADM) is designed using AA1, AA5, AA6, and AA7 in [40] for the image blending approach in image processing applications. An n-bit Wallace tree multiplier is designed using APAD adders in [41] for image processing applications, neural network applications.

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Another important block of digital signal processing is the FIR filter which is utilized in many applications of signal processing. Approximate adders can be used in the design of the FIR filter [46] for power-efficient DSP applications. A DCT block is designed using approximate adders in [24] which is used in image compression applications.

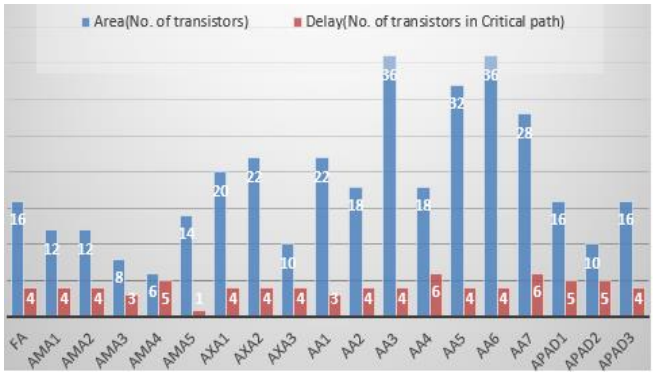

Fig. 2. Area and delay Comparison of adders

VI. CONCLUSION AND FUTURE SCOPE

In this review, 19 various categories of approximate adders of four dissimilar design categories are reviewed and analyzed. All the adders are analyzed based on area, delay, and accuracy. Also, reviewed adders are compared with accurate FA. When compared with FA, the discussed approximate adders in section 3 have very much less delay and the area is also less, but accuracy is low. From the result analysis section, it can be said that for some adder circuits as area decrease accuracy % decrease which is not desirable. From table 4, it is clear that most of the adders having the same delay. But area and accuracy level are changing for adder circuits. So, it can be said that all the approximate adders are fast in nature with different areas and accuracy levels. Depending on the type and requirement of the application any of the analyzed adders can be chosen.

If accuracy is important in design, then approximate adders with more are chosen and if area constraint is important, then an adder with less accuracy is chosen as it had less area. Considering the fact of accuracy to be at most priority, hence it can be said that AMA2, AXA2, AA5, and APAD2 are the finest adders when related to other approximate adders on basis of area, accuracy, and delay. All the analyzed approximate adders are single bit adders. Using these single bit adders, one can design adders of multiple bits and check for the enhancement in accuracy parameter

Table- II: The truth table of Full Adder and AAs (Note: Error denoted by X)

INPUTS			OUTPUT															
			FA		AA1		AA2		AA3		AA4		AA5		AA6		AA7	
A	B	CIN	S	Cout	S	Cout	S	Cout	S	Cout	S	Cout	S	Cout	S	Cout	S	Cout
0	0	0	0	0	1X	0	0	0	0	0	1X	0	1X	0	1X	0	0	0
0	0	1	1	0	1	0	1	0	1X	0	1	0	1	0	1	0	1	0
0	1	0	1	0	1X	0X	1X	0	0X	0	1	0	1X	0	1	0	1	0
0	1	1	0	1	1X	0X	1X	1	1X	1	0	1	1X	1	0	1	0	1
1	0	0	1	0	0	1	0	0	0	0	1	0	0	0	1	0	1	0
1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1
1	1	0	0	1	0	1	0	1	0	1	0	1	0	1	0	1	1X	1
1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0X	1	1	1

Table- III: The Logic table of APADs and Full adder (Note: Error denoted by X)

INPUTS			OUTPUT									
			FA		APAD1		APAD2		APAD3		APAD4	
A	B	CIN	S	Cout	S	Cout	S	Cout	S	Cout	S	Cout
0	0	0	0	0	0	0	0	0	0	0	0	0
0	0	1	1	0	1	0	1	0	1	0	0X	0
0	1	0	1	0	0X	1X	1	0	1	0	1	0
0	1	1	0	1	0	1	1X	0X	1X	0X	1X	0X
1	0	0	1	0	1	0	0X	1X	0X	1X	0X	1X
1	0	1	0	1	0	1	0	1	0	1	0	1
1	1	0	0	1	0	1	0	1	1X	1	1X	1
1	1	1	1	1	1	1	1	1	1	1	1	1

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Table- IV: Area Calculation of Approximate Adders

Type of Approximate Adder	Output equation with its literals	Principle of Area calculation		
		No. of literals in S and Cout equation	No. of inverters required	Total no. of transistors
AMA1	$S = (AB + \overline{Cout})Cin \ \& \ Cout = ACin + B$	7	1	16
AMA2	$S = \overline{Cout} \ \& \ Cout = AB + (B + A)Cin$	5	1	12
AMA3	$S = \overline{Cout} \ \& \ Cout = ACin + B$	5	1	12
AMA4	$S = (AB + \overline{Cout})Cin \ \& \ Cout = A$	3	1	8
AMA5	$S = B \ \& \ Cout = A$	2	1	6
AXA1	$S = Cin \ \& \ Cout = (A + B)\overline{Cin} + AB$	6	1	14
AXA2	$S = \overline{AB} + AB \ \& \ Cout = AB + (B + A)Cin$	9	1	20
AXA3	$S = (\overline{AB} + AB)Cin \ \& \ Cout = AB + (B + A)Cin$	10	1	22
AA1	$S = \overline{A} + BCin \ \& \ Cout = A$	4	1	10
AA2	$S = (\overline{A}(B + Cin) + BCin) \ \& \ Cout = AB + (B + A)Cin$	10	1	22
AA3	$S = (\overline{A} + B)Cin \ \& \ Cout = AB + (B + A)Cin$	8	1	18
AA4	$S = (\overline{A + Cin})\overline{B} + (ACin + \overline{ACin})B \ \& \ Cout = AB + (B + A)Cin$	13	5	36
AA5	$S = \overline{A} + BCin \ \& \ Cout = AB + (B + A)Cin$	8	1	18
AA6	$S = \overline{A}(\overline{B} + \overline{Cin}) + \overline{A}B\overline{Cin} \ \& \ Cout = AB + (B + A)Cin$	11	5	32
AA7	$S = AB + B\overline{Cin} + (\overline{A}Cin + \overline{ACin})\overline{B}$ $Cout = AB + (B + A)Cin$	14	4	36
APAD1	$S = ABCin + (\overline{A}\overline{B} + \overline{A}\overline{B})\overline{Cin} \ \& \ Cout = B + ACin$	11	3	28
APAD2	$S = \overline{A}B + (B + \overline{A})Cin \ \& \ Cout = A$	6	2	16
APAD3	$S = \overline{A}Cin + B \ \& \ Cout = A$	4	1	10

Table- V: Area, delay, and accuracy of Approximate Adders

Type of Approximate Adder	Area (No. of transistors)	Delay (No. of transistors in Critical path)	No of Errors	Accuracy (%)
FA	**16**	**4**	**0**	**100**
AMA1	**12**	**4**	**3**	**81.25**
AMA2	**12**	**4**	**2**	**87.5**
AMA3	**8**	**3**	**3**	**81.25**
AMA4	**6**	**5**	**5**	**68.75**
AMA5	**14**	**1**	**6**	**62.5**
AXA1	**20**	**4**	**8**	**50**
AXA2	**22**	**4**	**4**	**75**
AXA3	**10**	**4**	**2**	**87.5**
AA1	**22**	**3**	**5**	**68.75**
AA2	**18**	**4**	**2**	**87.5**
AA3	**36**	**4**	**3**	**81.25**
AA4	**18**	**6**	**1**	**93.75**
AA5	**32**	**4**	**3**	**81.25**
AA6	**36**	**4**	**2**	**87.5**
AA7	**28**	**6**	**1**	**93.75**
APAD1	**16**	**5**	**2**	**87.5**
APAD2	**10**	**5**	**4**	**75**
APAD3	**16**	**4**	**5**	**68.75**

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