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Design SSTL based Arithmetic Logic Unit for Internet of Things Based Processor

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Abstract*: *Now days in area of computer science Green computing is creating revolution by bringing some new digital component with less power consumption. Our research work is created on this idea. In this paper our objective is to come up with High Performance ALU design for IOT based processor by reducing the power consumption. For calculating total power consumption of FPGA based ALU we used five different voltage (0.95,1.0,1.05,1.10,1.15,1.20) and calculated IOs, Leakage power at four different IOs standard (SSTL18_II, SSTL15, SSTL135, SSTL15_R). In experiment we found the best result with SSTL15_R IO standard. We think that the application of this design will definitely help to design in futuristic IOT based processor development.

Keywords*: *ALU, SSTL, Verilog, RTL, SSTL18_II, SSTL15, SSTL135, SSTL15_R

I. INTRODUCTION

When we are talking about any technology then the design and implementation of FPGA-based Arithmetic Logic Unit (ALU) is of prime importance because ALU is an integral part of the Central Processing Unit(CPU). It is a combinational logic unit and a fundamental component of a microprocessor that conducts arithmetic and logic operations. Figure 1 shown Top Level of Schematic of Arithmetic Logic Unit.

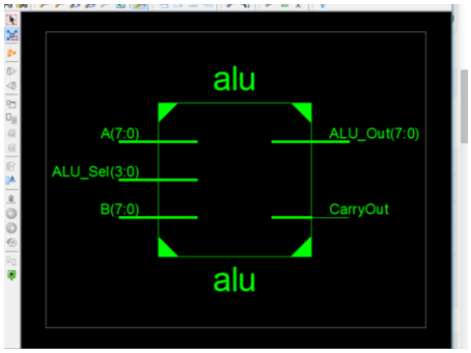

Fig.1 Top Level of Schematic of Arithmetic Logic Unit

Viewing an RTL schematic opens an NGR file that can be viewed as a gate-level schematic. This schematic is generated after the HDL synthesis phase of the synthesis process. It shows a representation of the pre-optimized design in terms of generic symbols, such as adders, multipliers, counters, AND gates, and OR gates, that are independent of the targeted Xilinx device. Figure2 shown RTL Schematic of Arithmetic Logic Unit.

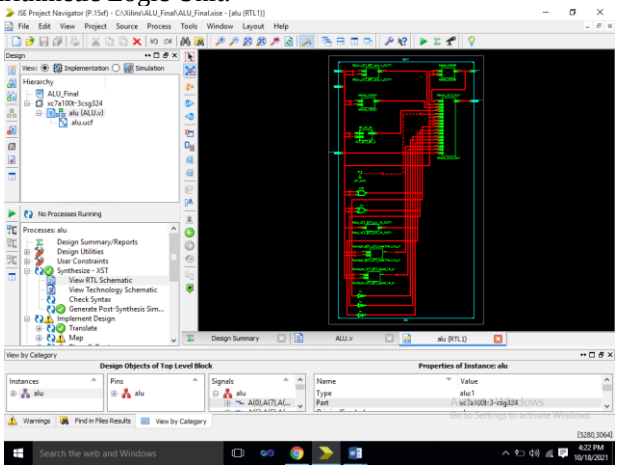

Fig.2 RTL Schematic of Arithmetic Logic Unit

A. ALU for IOT devices

ALUs are now becoming smaller and more advanced in order to allow the developer for the development of even much more powerful but compact systems and processors. In today's Internet of Things (IOT) devices, ALUs are extremely powerful and complicated, with a single unit containing multiple ALUs. While designing ALU for IOT devices, designing components to achieve low power constraints is of core significance.

B. Stub Series Terminated Logic

SSTL which stands for Stub Series Terminated Logic is a group of electrical standards for carrying an alternating current of radio frequency where wave nature must be taken into consideration for currents with high frequency. SSTL I/O standards used for general purposes are SSTL18 for 1.8V, SSTL15 for 1.5V, and SSTL135 for 1.35V.

II. LITRECHER REVIEW

Energy Efficient Solar Charge Sensor Design Using Spartan-6 FPGA [1], High Performance FIFO Design for Processor through Voltage Scaling Technique [2], An Integrated Maximum Power Point Tracker for Photovoltaic Panels. [3], Capacitance Scaling Based Low Power Comparator Design on 28nm FPGA [4] SSTL Based Energy Efficient FIFO Design for High Performance Processor of Portable Devices [5]. Energy Efficient CRC Design for Processor of Workstation, and Server using LVCMOS [6].

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Test of RAM-Based FPGA: Methodology and Application to the Interconnect [7] Block RAM-based architecture for real-time reconfiguration using Xilinx R FPGAs [8]. Techniques and Algorithms for Fault Grading of FPGA Interconnect Test Configuration [9]. Techniques and Algorithms for Fault Grading of FPGA Interconnect Test Configuration [10]. 8-bit AES FPGA Implementation using Block RAM [11].

III. WORKING METHODOLOGY

In the design methodology of FPGA based ALU first step is logic synthesis which is a process of abstract specification of circuit behavior, second step is technology mapping which is a process to convert logic gates to comprising logic cells on the target FPGA devices, third step is a placement which assign the nets to the routing segment, fourth step we always perform routing for the design and in last step bit file is generated which contain the programming information for an FPGA. The whole process of design methodology is discussed in figure 5.

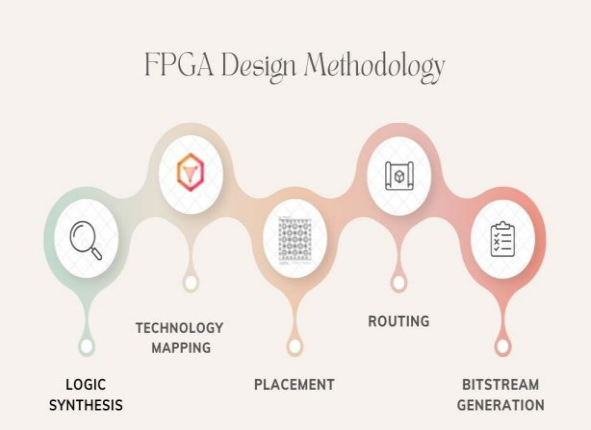

Fig.5 working methodology for designing ALU

IV. RESULT AND ANALYSIS

In table 1 we have worked with SSTL18_II IO standard to compute the total power consumption. During the analysis we found the major change in Leakage power while changing the voltage from 0.95 to 1.20 Volt

Table 1. Power consumption using SSTL18_II

Voltage	Leakage Power	IO Power	Total Power
.95	0.040 W	0.076W	0.116W
1.0	0.043 W	0.076 W	0.119 W
1.05	0.046 W	0.077W	0.122 W
1.10	0.049 W	0.077 W	0.126 W
1.15	0.054 W	0.077 W	0.131 W
1.20	0.059 W	0.078 W	0.136 W

During the bar analysis we have found no change in IO power. Total power has been changed around 17.24% when voltage has been changed from .95 to 1.20 volt. Same analysis has been shown by figure 5 using bar graph.

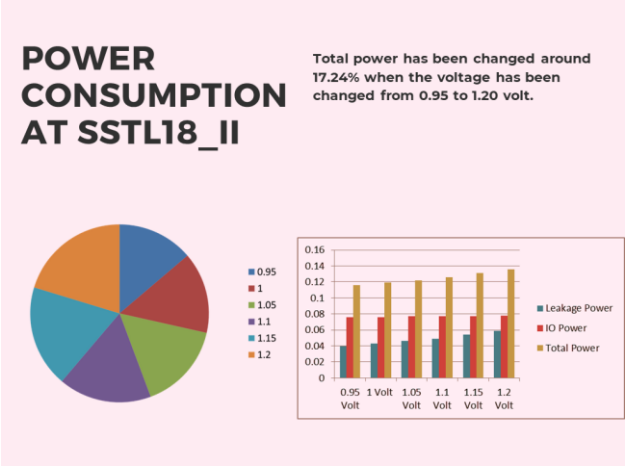

Figure6: Power consumption using SSTL18_II

In table 2 analysis has done with SSTL15 IO standard which is comes under the family of Stub-Series Terminated Logic. SSTL15 is used for DDR3 SDRAM interfaces and is roughly defined (not by name) in the JEDEC standard JESD79-3E. For this standard, the full-strength driver (SSTL15) is available in both the HP and HR I/O banks Same analysis has been represented by using bar graph in figure 6.

Table 2. Power consumption using SSTL15

Voltage	Leakage Power	IO Power	Total Power
.95	0.040W	0.058 W	0.098 W
1.0	0.042 W	0.059 W	0.101 W
1.05	0.045 W	0.059 W	0.104 W
1.10	0.049 W	0.059 W	0.108 W
1.15	0.053 W	0.059 W	0.113 W
1.20	0.058 W	0.060 W	0.118 W

In this analysis we found that total power consumption is directly proportional to voltage, when we increase the voltage from 0.95 to 1.20 the total power consumption is increased by 20.40%. Same analysis has been represented by using bar graph in figure 7.

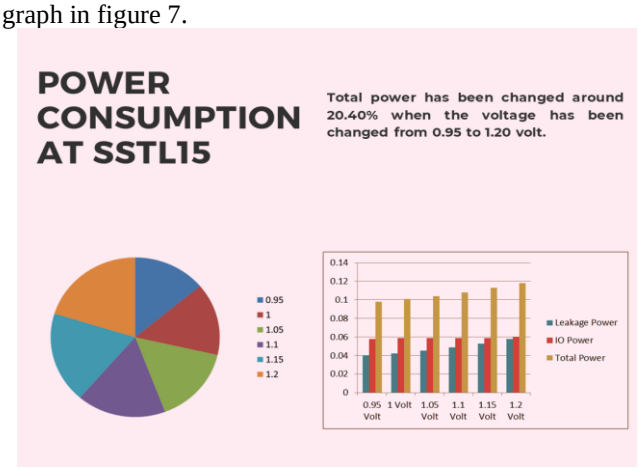

Figure7: Power consumption using SSTL15

In table3 total power consumption is computed with SSTL 135 IO standard. SSTL135 is used for DDR3L SDRAM interfaces and is roughly defined (not by name) in the JEDEC standard JESD79-3-1.

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During the analysis IO power is range bound under 0.056 to 0.057 but there is significantly change in leakage power from 0.039 to 0.058.

Table 3. Power consumption using SSTL135

Voltage	Leakage Power	IO Power	Total Power
.95	0.039 W	0.056 W	0.095 W
1.0	0.042 W	0.056 W	0.098 W
1.05	0.045 W	0.056 W	0.102 W
1.10	0.049 W	0.057 W	0.106 W
1.15	0.053 W	0.057 W	0.110 W
1.20	0.058 W	0.057 W	0.115 W

With SSTL135 IO standard when voltage has been changed from .95 to 1.20 volt then power is increased by 21.05%. The whole analysis also represented by using bar graph by figure 8.

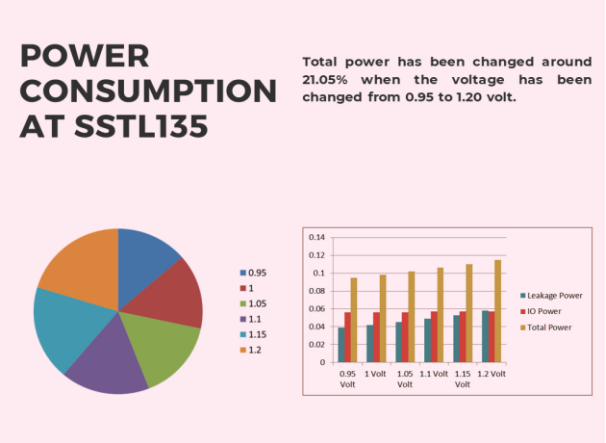

Figure 8: Power consumption using SSTL135

In table 4 sstl15_r io standards is used for the analysis which is a weaker, reduced-strength driver, designated by an r in the standard name (sstl15_r), is available in the hr i/o banks.

Table 4. Power consumption using SSTL15_R

Voltage	Leakage Power	IO Power	Total Power
.95	0.040 W	0.049 W	0.089 W
1.0	0.042 W	0.050 W	0.092 W
1.05	0.045 W	0.050 W	0.095 W
1.10	0.049 W	0.050 W	0.099 W
1.15	0.053 W	0.050 W	0.104 W
1.20	0.058 W	0.051 W	0.109 W

While working with SSTL15_R IO standard we found IO power value move within a range from 0.049 to 0.051 which indicate slightly static value. But found major change in leakage power. Leakage power is change 45% when we manipulate the voltage from .95 volt to 1.20 Volt. Due to voltage change we found 22.47% increment in total power consumption. Figure 9 shown the same analysis with the help of bar graph and pie chart.

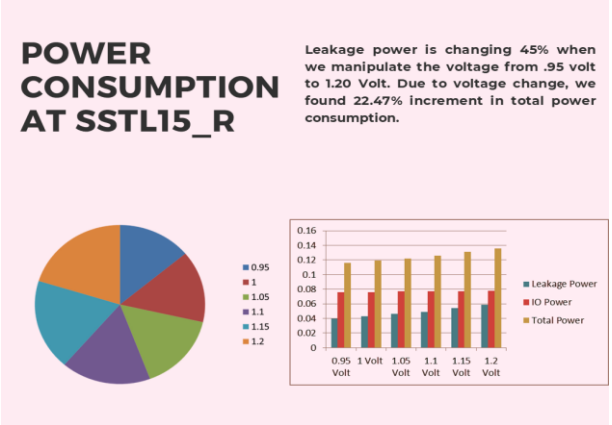

Figure 9: Power consumption using SSTL15_R

V. CONCLUSION

In this research work four Io standard has been used SSTL18_II, SSTL15, SSTL135 and SSTL15_R to design energy efficient FPGA based ALU. For analysis voltage scaling technique has been used(range 0.95 to 1.20 volt). During the whole analysis it found that SSTL15_R is most suitable for our FPGA device because at every voltage point it having less total power consumption.

FUTURE SCOPE

Here we have designed our RAM on 28nm FPGA but in future we have scope to redesign it on 16nm ultra scale FPGA. In this work we have used SSTL IOs standard but further we can use other IOs standard like LVCMOS or HSTL.

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