Performance Analysis of CMOS Circuits using Shielded Channel Dual Gate Stack Silicon on Nothing Junctionless Transistor

S.C. Wagaj, S.C. Patil

Abstract: In this paper it has been demonstrated that a shielded channel made by varying the side gate length in silicon-on-nothing junctionless transistor not only improves the short channel effect but also improve the performance of CMOS circuits of this device. The proposed device shielded channel dual gate stack silicon on nothing junctionless transistor (SCDGSSONJLT) drain induced barrier lowering (DIBL), cut-off frequency and subthreshold slope are improved by 20%, 39% and 20% respectively over the single material gate silicon on insulator junctionless transistor (SMG SOIJLT). The proposed device CMOS inverter full time $T_f$ (ps) and noise margin improves by 50% and 10% compare to shielded channel silicon on insulator junctionless transistor (SCSOIJLT). It has been observed that circuit simulation of CMOS inverter, NAND and NOR of proposed device. The static power dissipation in the case of proposed SCDGSSONJLT device are reduced by 45%, 81% and 83% respectively over the SMGSOIJLT. Thus, significant improvement in DIBL, cut-off frequency, propagation delay and static power dissipation at low power supply voltage shows that the proposed device is more suitable for low power CMOS circuits.

Keywords: Shielded channel, junctionless transistor, dual gate stack, silicon on nothing, NAND gate, NOR gate.

I. INTRODUCTION

This International technological road map for semiconductor nanoscale with junction transistor’s shallow junction formation is very challenging in fabrication. Author colinge et.al have introduced junctionless transistor with uniform doping of source, channel and drain region [1]. The electric field perpendicular to the channel is significantly very low in junctionless transistor means mobility degradation is very less [2][3]. However, in junctionless transistor improving the current driving capability and gate control on channel potential are the challenges in this device. To overcome the short channel effect problem related with nanoscale junctionless transistor, double gate junctionless transistor can be considered [4][8].

It has been observed that bulk planner junctionless transistor [6] and junctionless double gate transistor are having low leakage current due to high channel doping. Moreover, due to high channel doping the mobility reduces due to ionization scattering and subsequently results in lower transconductance [6][7]. To overcome these challenges, many authors have introducing solutions such as junctionless nanowire transistor with a dual material gate [8], dual material gate junctionless transistor with high-k spacer [9], dual material gate silicon on nothing junctionless transistor [10], dual material double gate junctionless transistor considering fringing field [11], charge plasma based transistor with induced graded channel [12], gate-all-around junctionless transistor [13], non-uniformly doped symmetric double gate junctionless transistor [14], have been proposed. Among these junctionless transistor and architecture, dual material double gate junctionless transistor is best candidate for CMOS logic circuits [15]. However, it has been observed that
dual material double gate with high-k spacer leads to an increase in gate capacitance and decrease in cut-off frequency [9]. Along with increases in device parameter fluctuations limits the scalability of junctionless transistor is the short channel effect. DIBL effect problem and excess parasitic capacitance arrive in SOI MOSFET due to charge accumulated in the thick buried layer. Air is insulating layer dielectric constant is unity. Buried oxide layer is removed by air and a structure is proposed as silicon-on-nothing MOSFET. Parasitic capacitance values between source/drain and substrate are induced in the silicon on nothing (SON) structure, and therefore a higher circuit speed can be expected with SON device [16]. Due to double layer gate stack design the output characteristics are improved. The drain bias variations and enhanced and the gate control on the channel charge is increased. The channel length of the proposed work 20nm [17], to reduce device gate leakage current and low off state current requirements the high-k dielectric is as an alternative to SiO2. The concept of double layer gate stack and silicon on nothing has been studied on various device architecture such as dual material double layer gate stack SON MOSFET [18], dual material double gate SON MOSFET [19], High-k gate stack properties in SON MOSFET, dual material double layer gate stack junctionless transistor [20]. Amin s and Sarin R.K. et.al demonstrate doping less dual material and gate stack architecture of junctionless transistor with high-k spacer and misaligned double gate JLT [21][22]. Although the concept of double layer gate stack SON has been widely studied on various device architectures, the effect of two layer gate stack and SON junctionless transistor for CMOS circuit has not been reported in earlier literature to the best of my knowledge. In our earlier work shielded channel junctionless transistor was proposed by reducing the short channel effects. Here the reduced DIBL effect was observed by varying side gate length and increased ON current due to workfunction difference of side gate [15].

In this paper, we demonstrate CMOS circuit implementation using N and P channel SCDGSOIJLT. A comparison of SCDGSOIJLT with SMG SOI JLT and SCJSOIJLT is performed. Performance parameters such as static power dissipation, propagation delay, noise margin, rise and fall time of CMOS inverter, NAND and NOR are thoroughly investigated. For the simulation COGENDA TCAD tool is used.

This paper is arranged as follows. Section II consist device structure and their dimensions used for simulation are presented. The methodology is also highlighted. The result and discussion are given in section III. Conclusion is presented in section IV.

## II. DEVICE STRUCTURE AND SIMULATION

Six different types of MOSFETs are used to implement CMOS circuits in this paper: namely, p- and n-channel SCDGSOIJLT and p- and n-channel SMGSOIJLT and p- and n- channel SCJSOIJLT. The schematic device structure of the SCDGSOIJLT is shown in Figure 1. Performance analysis for CMOS inverters is done for three different channel length 20nm, 30nm and 40nm as per the international technology roadmap for semiconductors (ITRS) [19]. The parameters considered for the simulation are main gate 4.77eV, side gate 4.5eV, channel donor doping N_D=0.4x10^{18} cm^{-3}, channel thickness t_c=10nm, gate oxide thickness 3nm (1nm SiO_2 and 2nm HfO_2), substrate doping N_A=1x10^{16} cm^{-3} respectively. A buried oxide thickness (t_{box}) is of 10nm (two oxide layer 2nm each and air thickness 6nm). Table 1 Device parameters used in simulation summarizes device parameters used in this simulation.

<table>
<thead>
<tr>
<th>Table1: Device parameters used in simulation</th>
</tr>
</thead>
<tbody>
<tr>
<td>Sr. No.</td>
</tr>
<tr>
<td>--------</td>
</tr>
<tr>
<td>1</td>
</tr>
<tr>
<td>2</td>
</tr>
<tr>
<td>3</td>
</tr>
<tr>
<td>4</td>
</tr>
<tr>
<td>5</td>
</tr>
<tr>
<td>6</td>
</tr>
<tr>
<td>7</td>
</tr>
<tr>
<td>8</td>
</tr>
<tr>
<td>9</td>
</tr>
<tr>
<td>10</td>
</tr>
</tbody>
</table>

Genius uses the Kane’s model [23] to calculate the carrier generation by band-band tunnelling G_{BB}. The expression for the generation rate of for electrons and holes is as shown in equation 1

\[ G_{BB} = A_{BBTBT} \cdot \frac{E^2}{\sqrt{E_g}} \cdot \exp\left(-B_{BBTBT} \frac{E^{3/2}}{E}\right) \] (1)

Where- E is the magnitude of electrical field; E_g is the bandgap of the material, A_{BBTBT} and B_{BBTBT} are empirical fitting parameters.

The default values for silicon are:

\[ A_{BBTBT} = 3.500000E+21 \]
\[ B_{BBTBT} = 2.250000E+07 \]

Lombardi Surface Mobility Model

The Lombardi mobility model [24] is an empirical mobility model shown in equation 2. The mobility model consist three different components as like surface roughness, phonon scattering and doping dependent mobility model. Bulk mobility model in Lombardi mobility model is similar to masetti’s model.
\[ \mu_b = \mu_0 \exp \left( -\frac{P}{N_{tot}} \right) + \frac{\mu_{\text{max}} - \mu_0}{1 + \left( \frac{N_{tot}}{C_r} \right)^\alpha} - \frac{\mu_I}{1 + \left( \frac{C_r}{N_{tot}} \right)^\beta} \] (2)

\[ \mu_{\text{max}} = \mu_2 \left( \frac{T}{300} \right)^\gamma \]

\[ \alpha = 0.680, \beta = 2.0, \xi = 2.5, \mu_0 = 52.2 \text{cm}^2/\text{Vs}, \]
\[ \mu_2 = 1417 \text{cm}^2/\text{Vs}, C_s = 3.43 \times 10^{10} \text{cm}^{-3}, C_r = 9.68 \times 10^{16} \text{cm}^{-3} \]

Carrier recombination, generation model, Fermi Dirac statics and impact ionization models and Lombardi mobility model in COGENDA TCAD. The quantum confinement model also have been incorporated in the simulation.

III. MODEL CALIBRATION

To ensure the validity of results, initially calibration of simulation models is done with reference to simulation result of MOSFET characteristics presented in [9] and n-channel JLT [5]. Thus the model characteristic is shown in Figure 2 and Figure 3. There is good agreement of COGENDA TCAD simulated and simulated result of different researchers is evident in these figures.

IV. RESULTS AND DISCUSSIONS

1.1 Performance comparison of SCDGSSONJLT and SCSOIJLT

SCDGSSONJLT’s subthreshold slope, drain induced barrier lowering (DIBL) and cut-off frequency are improved by 20%, 20% and 39% respectively over the single material gate silicon on insulator junctionless transistor (SMG SOI JLT). The \( I_D - V_{DS} \) characteristics are shown in Figure 4. Figure 4 compares the transfer characteristics of n channel and p channel SCDGSSONJLT with SCSOIJLT. The main reason for this improvement is, reduction of the effective gate oxide of thickness of n type SCDGSSONJLT due to dual gate stack design (1.312nm). Output characteristics of n and p channel SCDGSSONJLT enhanced compare to SCSOIJLT at a fixed \( V_{GS} = 1.5 \text{V} \), work function main gate=4.9eV, side gate=4.17eV, \( N_D = 0.4 \times 10^{18} \text{cm}^{-3} \).

![Figure 4. \( I_D \) vs \( V_{DS} \) characteristics of shielded channel JLT and proposed n-channel and p-channel SCDGSSONJLT at different \( V_{GS} \) values](image)

Figure 4. \( I_D \) vs \( V_{DS} \) characteristics of shielded channel JLT and proposed n-channel and p-channel SCDGSSONJLT at different \( V_{GS} \) values

The electric field in the channel increase due to side gate biasing. Due to high electric field in the channel velocity of electron increases. The ON state current of SCSOIJLT is lower due to high doping density. In presence of the effect of using high- \( k/\text{SiO}_2 \) gate-stack architecture on the transfer characteristics of SCDGSSONJLT and SCSOIJLT. The advantage of gate stack in terms of increased \( I_{ON} \). ON current of SCDGSSONJLT is 45.4\( \mu \text{A} \) and for SCSOIJLT is 14.1\( \mu \text{A} \) at \( V_{GS} = V_{DS} = 1 \text{V} \).
Figure 5 shows that comparison of gate to drain capacitance $C_{gd}$ and gate capacitance $C_{gg}$ for n & p channel as a function of the gate-to-source voltage $V_{GS}$ between SCDGSSONJLT and SCSOIJLT. The gate capacitance $C_{gg}$ consist of the series combination of gate to channel capacitance and gate oxide capacitance.

Capacitance components $C_{gg}$, $C_{gs}$ and $C_{gd}$ have the relationship

$$C_{gg} = C_{gs} + C_{gd}$$

(3)

Gate oxide capacitance $C_{ox}$ can be evaluate as

$$C_{ox} = \frac{2\pi e L_g}{\ln(1 + \frac{\varepsilon_{ox}}{R})}$$

(4)

Table 2: Delay and static power dissipation of inverters

<table>
<thead>
<tr>
<th>$L_G$ In nm</th>
<th>$V_{DS}=1V$</th>
<th>$V_{DS}=0.5v$</th>
<th>$V_{DS}=1v$</th>
<th>$V_{DS}=0.5v$</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>$P_{static}$ (W)</td>
<td>$\tau_p$ (pS)</td>
<td>$P_{static}$ (W)</td>
<td>$\tau_p$ (pS)</td>
</tr>
<tr>
<td>20</td>
<td>7.82x10^{-10}</td>
<td>10</td>
<td>2.01x10^{-10}</td>
<td>50</td>
</tr>
<tr>
<td>30</td>
<td>3.37X10^{-11}</td>
<td>19</td>
<td>1.10x10^{-11}</td>
<td>20</td>
</tr>
<tr>
<td>40</td>
<td>3.21X10^{-12}</td>
<td>24</td>
<td>1.26x10^{-12}</td>
<td>20</td>
</tr>
</tbody>
</table>

In transient response gate capacitance role is very important. It is observed that $C_{gd}$ for the SCDGSSONJLT are lower than that for SCSOIJLT. In linear region 0.275fF capacitance at $V_{GS}=0.08v$ and $V_{DS}=1V$ for SCDGSSONJLT and 0.117fF capacitance at $V_{GS}=0.08v$ and $V_{DS}=1V$ for SCSOIJLT and in saturation region 0.2fF capacitance at $V_{GS}=V_{DS}=1V$ of SCDGSSONJLT and 0.1fF capacitance at $V_{GS}=V_{DS}=1V$ of SCSOIJLT.
Figure 6. Comparison of static power dissipation of a) CMOS inverter, b) NAND gate and c) NOR gate circuit based on SCSOIJLT and proposed SCDGSSON junctionless transistor at various channel lengths.

All the capacitances are simulated as simulation mode AC sweep at a frequency of 1MHz. The SCDGSSONJLT has highest $C_{gg}$ compared with SCSOIJLT. This is attributed to high-k gate stack.

Figure 6 shows the plot between static power dissipation v/s physical gate length for $V_{DS}=1V$ (LHS) and $V_{DS}=0.5V$ (RHS) for inverter, NOR and NAND gate. The channel length consider for this simulation are 20nm, 30nm and 40nm and side gate length is 10nm which is constant for SCDGSSONJLT and SCSOIJLT. It has been observed that OFF current of MOSFET as well as static power dissipation decreases due to high-k gate stack.

Table 2 summarize CMOS inverter $P_{\text{static}}$ and $\tau_p$ values for $V_{DS}=0.5V$ and 1V. At $V_{DD}=0.5V$ and channel length 30nm, 40nm of SCDGSSONJLT inverter static power dissipations are 11pW,
1.26pW respectively, and SCSOIJLT inverter static power is 14.7pW. The static power dissipation of SCDGSSONJLT NOR gate is 3.55pW at \( V_{DD}=0.5V \) and channel length of 40nm. The static power dissipation is 5.55pW for SCSOIJLT NOR gate. Static power dissipation of SCDGSSONJLT is minimum due to high phonon scattering below threshold voltage. Figure 7 shows the graph between propagation delay v/s physical channel length of SCDGSSONJLT and SCSOIJLT inverter, NAND and NOR gate. Propagation delay of SCDGSSONJLT is minimum as compared to SCSOIJLT. The delay time \( \tau_d \) is defined as \( \tau_d = (\tau_r + \tau_f)/2 \), where the rise time \( \tau_r \) and the fall time \( \tau_f \) are extracted at \( V_{out}=V_{dd}/2 \). Device aspect ratio of SCDGSSONJLT device is 50 because channel length is 20nm and width is 1μm. When Channel length increases then propagation delay of inverter SCSDGSSOJLT decreases and propagation delay of SCDGSSONJLT reduces by 20% as compared to SCSOIJLT. Propagation delay of SCSOIJLT is 110ps and proposed SCDGSSONJLT is 20ps at \( V_{DS}=0.5V \) at channel length 40nm. SCDGSSONJLT NOR gate propagation delay is improved by 22%, 45% and 52% over the SCSOIJLT at channel length 20, 30 and 40nm respectively at \( V_{DS}=0.5V \). Proposed SCDGSSONJLT is best candidate for low power CMOS circuit.

Figure 8. Transient response of CMOS inverter a) proposed SCDGSSONJLT b) SCSOIJLT at different side gate length.

Figure 8 a and b shows that the transient response of CMOS inverter SCDGSSONJLT and SCSOIJLT, it is useful for different side gate length calculation of propagation delay \( \tau_p \). Propagation delay indicates that time require by CMOS inverter to switch from OFF state to ON state. When propagation delay increases then lower will be the speed of device. It has been observed that SCDGSSONJLT exhibits smallest propagation delay of 20pS and SCSOIJLT has larger propagation delay that is 30pS. Voltage overshoot and undershoot effect leads in the transient response due to \( C_{gd} \). In SCSOIJLT the undershoot peak arises due to the larger \( C_{gd} \). Table 3 summarizes transient response inverters for different side gate lengths at \( V_{DS}=1V \). SCDGSSONJLT and SCSOIJLT inverters rise time \( (\tau_r) \) and fall time \( (\tau_f) \) are calculated from transient characteristics at a different side gate channel length as shown in table 3.

Figure 9. Comparison of a) Subthreshold swing, b) drain induced barrier lowering with physical channel length of SCDGSSON and SMGSOI n-channel and p-channel junctionless transistor at \( V_{SGS}=1.5V \).

If SCDGSSONJLT side gate length increases from 10nm to 20nm then current is remains constant, hence rise time also remains constant. The side gate length increases from 20nm to 30nm then...
Table-4 Device parameters for different channel length

<table>
<thead>
<tr>
<th>Channel length (nm)</th>
<th>V_DS(V)</th>
<th>SCDGSSONJLT n-type</th>
<th>SCDGSSONJLT p-type</th>
<th>SMGSOIJLT n-type</th>
<th>SMGSOIJLT p-type</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>V贷 (μA)</td>
<td>V贷 (mV)</td>
<td>V贷 (μA)</td>
<td>V贷 (mV)</td>
<td>I贷 (μA)</td>
</tr>
<tr>
<td>20</td>
<td>45.4</td>
<td>410</td>
<td>-</td>
<td>-</td>
<td>83.7</td>
</tr>
<tr>
<td>20</td>
<td>11.7</td>
<td>680</td>
<td>-</td>
<td>-</td>
<td>51.3</td>
</tr>
<tr>
<td>30</td>
<td>78.4</td>
<td>430</td>
<td>17.1</td>
<td>1150</td>
<td>71.9</td>
</tr>
<tr>
<td>30</td>
<td>36.6</td>
<td>550</td>
<td>4.8</td>
<td>1500</td>
<td>20.3</td>
</tr>
<tr>
<td>40</td>
<td>74.3</td>
<td>510</td>
<td>17</td>
<td>1140</td>
<td>79.4</td>
</tr>
<tr>
<td>40</td>
<td>34.6</td>
<td>780</td>
<td>4.7</td>
<td>1210</td>
<td>31.9</td>
</tr>
</tbody>
</table>

Channel potential shift away from main channel length. The current driving capability decreases then rise time increases from 10ps to 20ps and side gate length increases from 30nm to 40nm then drain current is remains constant means rise time remains constant. It is observe in τr for SCDGSSONJLT is lower than that of SCGSOIJLT at side gate length of 20, 30 and 40nm. It has been observed that rise time of both inverter remains constant. Figure 10 shows that voltage transfer curve (VTC) of CMOS inverter with SCDGSSONJLT is approximately similar to CMOS inverter with SCSOIJLT having the same effective channel length i.e. L=20nm. Figure 10 shows that noise margin is calculated from Figure 9b, shows the graph between sub-threshold slope (SS) and physical gate length for PMOS and NMOS. The physical gate length and Figure 9a shows a graph between subthreshold slope (SS) and channel length 30nm is 0.36V in high state. Noise Margin at channel length 30nm is 0.32V and SCSOIJLT is 0.34V. Noise Margin at channel length 40nm is 0.32V and SCSOIJLT is 0.34V. Noise Margin at high state (NM_H) of SCDGSSONJLT is 0.39V and SCSOIJLT is 0.34V. Noise Margin at high state (NM_H) of SCDGSSONJLT is 0.32V and SCSOIJLT is 0.39V where NM_H and NM_L are calculated using following equation. Noise margin at channel length 30nm is 0.36V in high state and 0.37V in low state.

\[ NM_H = V_{OH\min} - V_{I\min} \]
\[ NM_L = V_{OL\max} - V_{IL\max} \]

1.2 Comparison of SCDGSSONJLT and SMGSOIJLT

Multi material gate junctionless transistor improves the performance as compared to single material gate junctionless transistor. The different researchers demonstrates that multi material gate junctionless transistor is best candidate for CMOS design compare to single material gate junctionless transistor [9] [16]. In this section multi material gate SCDGSSONJLT’s CMOS circuits logical performance compared with single material gate junctionless transistor. Figure 9a shows a graph between subthreshold slope (SS) and physical gate length and Figure 9b shows the graph between DIBL and physical gate length for PMOS and NMOS. The DIBL is calculated from equation 5,

\[ DIBL = \frac{V_{TLIN} - V_{TSAT}}{0.95} \]

Where \( V_{TLIN} \) is threshold voltage at \( V_{DS}=0.05V \) and \( V_{TSAT} \) as a threshold voltage at \( V_{DS}=1V \) and the poly gate work function is 4.77eV and n poly gate is 4.1eV. It can be seen that due to side gate biasing, the DIBL and SS are reduced for SCDGSSONJLT as compared to SMG SOI JLT NMOS and PMOS devices. It has been observed that n-channel SCDGSSONJLT, the DIBL and SS are 40mV/V and 90 mV/decade and for SMGSOIJLT DIBL and SS are 50mV/V and 90mV/decade. The P-channel SCDGSSONJLT DIBL is -70mV/V and for SMGSOIJLT is -60mV/V at channel length 40nm. The sub-threshold current, \( I_{sub} \) can be expressed in terms of \( V_{TSAT} \) and SS as shown in equation 6 [26].

\[ I_{sub} = I_0 \times 10^{(V_{TSAT}/SS)} \]
Figure 10. VTCs of CMOS inverter a) SCSOI b) proposed SCDGSSON junctionless transistor

\[ SS = \frac{KT}{q} \ln \left( 1 + \frac{1}{C_{ox1} \left( \frac{C_{si}}{C_{si}} + \frac{C_{ox2}}{C_{ox2}} \right)} \right) \]  

(7)

$C_{ox1}$ is gate capacitance and $C_{ox2}$ is buried oxide capacitance and $C_{si}$ is body channel capacitance \( C_{si} = \varepsilon_{si}/t_{si} \).

Figure 11. VTC for SCDGSSONJLT and SCOSOIJLT for channel length 20nm

Figure 12 shows the voltage transfer characteristics and short circuit current \( I_{SC} \) of Inverter with SCDGSSONJLT and SMGSOIJLT inverter for supply voltage of \( V_{dd}=1V \). The SMG SOI JLT inverter shows lower noise margin and higher short circuit current as compare to SCDGSSONJLT, which is related to the ON current properties of these devices. Short circuit current of SMGSOIJLT is maximum compared to SCDGSSONJLT. 23.7\mu A short circuit current of SCDGSSONJLT and 25.8\mu A of SMGSOIJLT and hence short circuit power dissipation of SMGSOIJLT is maximum compared to SCDGSSONJLT.

Figure 13. Comparison of static power dissipation of CMOS inverter, NAND gate and NOR gate circuit based on SMG SOI and proposed SCDGSSON junctionless transistor at various channel length.
Figure 13. shows the comparison of static power dissipation of CMOS NAND and proposed SCDGSSONJLT. The significant reduction in both $P_{static}$ and $r_p$ at minimum supply voltage observe the suitability of the proposed SCDGSSONJLT for low power CMOS logic circuits. At $V_{DS}=0.5V$, the SCDGSSONJLT inverter static power dissipation is 0.6nW and that of SMGSOIJLT inverter is 4.7nW. The SCDGSSONJLT NOR gate static power dissipation is 1.73 nW and that of SMGSOIJLT is 4nW at channel length 20nm. The static power dissipation of SCDGSSONJLT NAND gate is 1.35 nW, and that of SMGSOIJLT is 1.78nW at channel length 30nm. It has been observed that SCDGSSONJLT logic gate has good performance at low power. Table 4 summarize the ON current and threshold voltage of n and p channel of SCDGSSONJLT and SMGSOIJLT. It has been observed that 44% maximum ON current of SCDGSSONJLT as compared to SMGSOIJLT at channel length 30nm. Maximum $\sigma V_{th}$ of n channel SCDGSSONJLT is 370mV and SMGSOIJLT is 380mV. Average threshold voltage for SCDGSSONJLT is 560mV and it is suitable for low power device at $V_{DS}=0.5V$. For SMGSOIJLT average threshold voltage is 386mV. The hole density and electric field distribution in the middle of the channel when device operated in the off-state. When device is in the off-state, the channel region to be almost completely depleted, the bulk conduction of holes is reduced. The hole mobility hovers around 40 cm$^2$/Vs. in p-type silicon for high doping concentration. The threshold voltage of p-type SCDGSSONJLT increases.

Where, $C_{gs}$ is gate capacitance and $g_m$ is transconductance. Due to higher current conductivity of SCDGSSONJLT at side gate length 40nm, the cut-off frequency $f_t$ is maximum than that of SMG SOI JLT and SCDGSSONJLT at side gate lengths of 10nm, 20nm and 30nm. The value of $f_t$ for SMGSOIJLT, SCDGSSONJLT are 300 GHz, 700 GHz respectively at $V_{GS}=0.6V$ and $V_{DS}=1V$ respectively. The value of SCDGSSONJLT increases due to dual gate stack gate material and in silicon on nothing technique no charge is accumulate in air. It has been observed that SCDGSSONJLT cut off frequency is improved as compared to SMGSOIJLT by 54%.

V. CONCLUSION

- The proposed device SCDGSSONJLT performs better than SMG SOI JLT. The subthreshold slope, DIBL, and cut-off frequency are improved by 20%, 20% and 39% respectively over the SMG SOI JLT.
- Three CMOS circuits have been proposed namely, Inverter, NAND and NOR gate
- The proposed device CMOS inverter fall time $T_f$ (pS) and noise margin are improved by 50% and 10% respectively, as compared to SMG SOI JLT
- The static power dissipation in proposed SCDGSSONJLT device is reduced by 45% ,81% and 83% respectively over the SMGSOIJLT at $V_{DS}=0.5V$.
- The improvement in Propagation delay of SCDGSSONJLT NOR gate at 20nm, 30nm and 40nm is 40%, 50% and 40% respectively, as compared to SCOIJLT.
- Although the lower gate capacitance in junctionless SCDGSSONJLT suppresses the undershoot effect in the circuit, the Cut off frequency of SCDGSSONJLT improves by 54% compared to SMGSOIJLT.

ACKNOWLEDGEMENT

This work has been funded by BCUD Savitribai Phule Pune University, Pune. Authors would like to thank VNIT Nagpur and Amit Saini for technical support.

REFERENCES

Performance Analysis of CMOS Circuits using Shielded Channel Dual Gate Stack Silicon on Nothing Junctionless Transistor


AUTHORS PROFILE

S.C.Wagaj, received the B.e.and M.E. degrees in Electronics Engineering from Shivaji University Kolhapur, Mahashtra, India, in 1999 and 2006 respectively. He has completed the Ph.D. with Modeling and simulation of junction-less transistor for low power and high performance in the JSPM’s Rajarshi Shahu college of Engineering Pune research center of Savitribai Phule Pune University, Pune. He is currently working as Assistant Professor at JSPM’s Rajarshi Shahu college of Engineering Pune. His research interests includes Modeling and Simulation of novel device structures on SOI Junction-less MOSFETs. He is a life member of Indian Society for Technical Education New Delhi India. He published five papers in International Journal and four papers in International Conference. He published one Indian patent on shielded channel junctionless Transistor in Jan 2016. Email: scwagaj@gmail.com

Shailaja Patil, is professor at the Department of Electronics and Telecommunication of RSCOE, affiliated to Savitribai Phule Pune University, Pune. She received Ph.D. in Computer Engineering from SVNIT, SURAT. She has total 25 years of research and teaching experience in the field of Wireless Technologies, Internet of Things and Pervasive computing. She has authored many research articles in International conference and journal, Book chapters, Patent, and Book. She has worked as session chair/ reviewer/ for various national/ international conferences. She is a member of professional bodies such as ISTE, IEEE and ACM. Email: shailaja.rscoe@gmail.com