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Review of CMOS Amplifiers for High Frequency Applications

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Abstract: ***The headway in electronics technology proffers user-friendly devices. The characteristics such as high integration, low power consumption, good noise immunity are the significant benefits that CMOS offer, paying many challenges simultaneously with it. The short channel effects and presence of parasitic which prevent speed pose questions on the performance parameters. A great sort of works has done by many groups in the design of the CMOS amplifier for high-frequency applications to discuss the parameters such as power consumption, high bandwidth, high speed and linearity trade-off to obtain an optimized output. A lot of amplifier topologies are experimented and discussed in the literature with its design and simulation. In this paper, the various efforts associated with CMOS amplifier circuit for high-frequency applications are studying extensively.***

Keywords*: CMOS (Complementary Metal Oxide Semiconductor), Operational Transconductance Amplifier (OTA), Phase Margin, UGB (Unity Gain Bandwidth).*

I. INTRODUCTION

In modern world markets for secured, portable and high-speed devices is growing. So to satisfy certain heighten interest technologies have also progressed quickly. This has also pointed to a notable efflorescence in the electronics area. Development of low power devices has to lead to emergency of handy or portable devices the downscaling of devices is happening so quick nowadays. The development of an Integrated circuit is one of the main reasons for the downscaling the device. CMOS amplifiers play a vital role in the field of communication. With each generation of CMOS technology, the decrease in supply voltage and transistor length continuously brings more complex issue for the design of the CMOS circuits. The CMOS amplifiers with different levels of complexity are used to realize functions ranging from dc bias generation to high-speed amplification or filtering. Rapid developments are going on in the RF communication field. The supreme necessity of the modern world is to complete a job efficiently and at high speed. Communication system plays an important part in increasing the speed and efficiency of many systems. Electronic devices such as mobile phones become an integral part of our day to day life. Due to the scaling and innovations in RF architectures, the cost of electronics goes down. Block diagram of an RF communication system is shown in Fig.1. In RF communication, amplifier circuits such as low noise amplifier, power amplifier, distributed amplifier and driver amplifier play a vital role. Now days a lot of research works being done in power amplifier and low noise amplifier. While designing a CMOS amplifier many points have to be noted to avoid unnecessary performance degradation. CMOS technology has very low power consumption so it can be used for this low power invented amplifier. CMOS is a MOSFET that has symmetrical and complementary pair of p and n-type MOSFET. The designer should deal with numerous tradeoffs among gain, bandwidth, power consumption, Noise etc. The improvement in all performance parameters simultaneously is a tedious task. So the designers are trying to keep a balance among the parameters. Many research works related to CMOS amplifier for high-frequency applications is going on during this period. In this paper detailed review on CMOS amplifiers for high-frequency applications has presented.

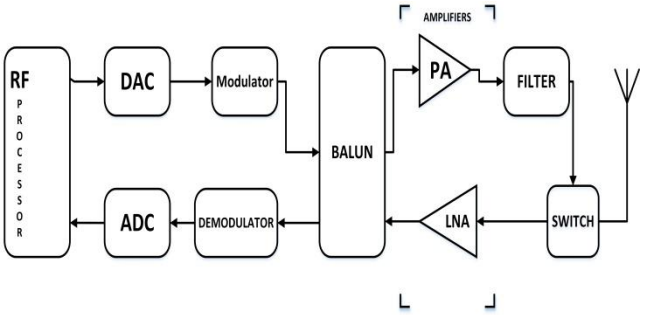

Fig.1 Block Diagram of RF Transceiver System

II. LITERATURE REVIEW

In 1976 ,YANNIS P TSIVIDIS et.al presented an internally compensated operational amplifier using n channel AI gate MOS technology[1]. In this work enhancement mode devices are used. Circuit is designed such that its performance is insensitive to process parameters. The realization of analog functions using this technology seemed to be more difficult. As circuit complexity level in a single chip increases, the partitioning of subsystems is difficult. This lead to implementation of different type in a single chip. This paper described internally compensated differential amplifier and it can be applicable in many analog digital MOS LSI circuits. This work concentrated on fast settling, low gain operational amplifier which could be used with capacitive loads. Frequency compensation was accomplished through a capacitance in source follower which is across cascode stage. The work used minimum feature size as 12µm and obtained the result as 5MHz UGB , 51dB gain, and with power consumption of 150mW.
In 1978,

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WOLFGANG STEINHAGEN et.al presented a single-stage differential amplifier in a standard metal gate process. In that article, the differential amplifier stage was compared with bipolar one.

The parameters like open-loop gain and the gain-bandwidth product achieved in this work were better over that of bipolar one. Here authors attempted to procure some design aspects for analogue CMOS circuits in nano ampere region. They achieved bandwidth of 500Hz.CMOS parts nourished to reduce power operation.[2]

JEAN –CLAUDE BERTAILS and the team discussed the calculation of equivalent input noise voltages of MOS amplifiers in three different technologies in 1979. Different means to reduce noise are also discussed in that paper. Here noise performance of CMOS amplifier, differential amplifier and push-pull amplifier are analyzed. To reduce noise, they tried to increase transistor length.[3]

Paul R Gray and et.al presented an overview of design technologies that existed during that period implemented in CMOS and NMOS technology in 1982[4]. Main importance was given to CMOS amplifiers due to their widespread use. Here the authors analyzed different performance parameters of CMOS implementation. A typical set of values with 4um silicon gate CMOS technology was described in this paper. With 5pF load capacitance, the unity-gain bandwidth frequency obtained was 4MHz. The paper described the scenario on that period about the variation of performance parameters such as open-circuit voltage gain, offset voltages, slew rate, power dissipation and noise performance on different device geometry and bias values. Frequency response and pole-zero locations on different capacitance and transconductance had discussed here. The significance of poles and zeros and the different means to eliminate the effect of right half-plane zero are summarized in this paper. The modification in the circuit with cascode or common source or common gate topology and its advantages are included in this journal. Different considerations for output amplifiers are narrated.

.In 1984, DAVID B RIBNER and group focused on power supply rejection problems and analyzed different cascode techniques. A folded cascode technique to get a wide common-mode input range is discussed in this paper. A detailed small-signal model for cascode amplifier is included in this paper and thereby the op-amp design is simplified here. The ac small-signal model for PSRR of internally compensated cascoded and non-cascodedopamp have been analyzed in this paper[5].

Here two circuits have been discussed such that the PSRR and Common-mode Input range is to be improved. The proposed circuits are for virtual ground applications and other for buffer applications. Here both type circuits and its results are well described along with its results.

In 1985, D.Ray and et.al extended the work of switched capacitor techniques using area-efficient transconductance amplifiers[6]. The amplifier presented in this paper comprised of a single gain stage with improved slew rate and unconditional stability. This work was simple and this simplicity allowed scaling in bias current and transistor geometry. The circuit was simulated with two load capacitors in pF range and the highest gain-bandwidth product obtained was with lowest load capacitor value. In the same year, J.A.Fisher proposed a CMOS Power Amplifier with new input stage with a modified class AB output stage [7]. Here the amplifier is fabricated using conventional silicon gate p well process. This work took the advantage of the common source output stage to get high load current capability with high output swing. A pseudo source amplifier formed by including local feedback network was discussed in previous literature which resulted in better voltage swing, reduced bandwidth and decreased stability. Also, different compensation methods have been trialled but faced difficulties such as poor supply rejection at high frequency, reduced common-mode range, degraded offset voltage. In this paper, a new input stage which manifested excellent supply rejection properties and improvement in gain is discussed. Along with the input stage, a varied output stage in which improved frequency response is included in the core amplifier which is proposed in this system. Here a three-stage core amplifier with wide bandwidth input stage and two high gain stages included a returning capacitor to virtual ground to improve power supply rejection. In this, the gain is improved significantly without sacrificing stability. With 5V power supply, the circuit exhibited 93 dB gain,1.2 MHz bandwidth with 12.7mW power dissipation.

In 1987 Marc.G.R.Degrauwe and team discussed a new design tool for the design of analogue circuit[8]. The manpower required for these designs has reduced with the help of the discussed tool. Along with IDAC overview, design steps, output results the program limitations are also discussed in this paper.

In 1988 G.Enpinosa and team presented noise performances of OTA-C filters along with its analytical expressions and simulated results [9].

F.O.Eynde and W.Sansen compared and optimized several CMOS amplifier prototypes for high-frequency applications in 1989. They derived scaling laws for power dissipation as a function gain-bandwidth product and load capacitance. In that paper, the authors presented 3 µm amplifier with 150MHz gain-bandwidth product,60o phase margin and 30mW power dissipation for 2pF load capacitance[10]

In the same year, R.A.Sartschev treated different analogue CMOS circuits such as IF amplifier, VGA, Switch and limiter. The 3 dB bandwidth of the intended amplifier is 437 MHz and its gain is 13.3 dB. In the design of VGA good output in terms of the gain-bandwidth product were acquired for gains 6 dB per each stage. The detailed small-signal analysis was performed to know back the different parameters in different above-mentioned circuits[11].

In 1990 G. O.Donoghue et.al discussed an amplifier using MOSFET with variable gain from 0dB to 42 dB[12]. Here the authors obtained fixed bandwidth at all closed-loop gains. In this work, a controlled PMOS active matrix is used to get constant phase and optimized noise, offset performance. Here eight such amplifiers are implemented in a single chip with more than 100 dB isolation. Also, different relationship graphs such as between gain and frequency, phase error and frequency, PSRR and frequency, cross talk and frequency & slew rate and gain are discussed in this work.

After a year T.Inoue and team suggested a new CMOS linear operational transconductance amplifier with wide input voltage range[13]. Here a bias current modulation based technique is utilised for linearization.

A source coupled NMOS transistor pair with a bias current source and simple PMOS current mirror load formed single-ended differential OTA. In this paper frequency response and dc transfer characteristics for different control, voltages are presented. Along with above-mentioned simulation results, the response of second-order OTA-C band bass filter with 3.58 MHz bandwidth is covered in this paper.

In the same year, R.E.Vallee and E.I.EI-Masry presented a design technique for high frequency switched capacitor applications[14]. The settling time was one of the important design constraints since it was for a switched capacitor application. The selection of a load capacitor was the difficult task due to the tradeoff between bandwidth, stability and settling time. In this work, a predefined layout-block which can be placed side by side is used to minimize settling time. The effect of proposed topological scaling of transistors for new load capacitance value optimized the settling time.

In 1993 P.J.Crawley and G.W.Roberts used a generalized high swing cascoded current mirror instead of standard cascoded current mirror to improve output voltage range with low voltage supply. With the proposed generalized scheme one can build multiple cascoded OTA with a larger bandwidth[15]. In that paper, single and double cascoded current mirrors are compared and the authors found that the double cascoded current mirrors exhibited better gain-bandwidth product than single cascode current mirror. Here the supply voltage used is 3.3V and the output voltage range obtained was 2V.

In next year Anchada and et.al presented an operational transconductance amplifier using Bi CMOS for high-frequency mixed-signal applications[16]. This circuit exhibited very linear broad dynamic range performance parameters. The MOSFET, BiCMOS and bipolar conversion stages are compared in this paper. The frequency compensation techniques along with circuit frequency response are analyzed in this work.

In 1995 E.Abou-Allam and E.I.El-Masry proposed a new design technique to improve frequency characteristics of the current amplifier. Here current steering is used to increase non-dominant pole and thereby unity-gain bandwidth[17]. In this work, the current operational amplifier is divided into three stages namely trans-impedance stage, transconductance stage and auxiliary voltage amplifier stage. A cascode structure is used there to implement trans-impedance stage and this improved current gain of the proposed system. They used the tool HSpice for simulation. The described single input differential output current amplifier is modified for differential input operation. Here the transistors are modelled using Level 2 parameters of Northern Telecom's 1.2µm CMOS process. This circuit exhibited dc gain of 64dB, the bandwidth of 100KHz, unity-gain bandwidth of 200MHz, phase margin of 60o and 5µs settling time. The circuit consumed 2.5mW power from ±3V power supply.

In 1996 Jean-Paul E and team used early voltage and gm/Id as a design parameter in this paper[18]. The dependence of these parameters on temperature is discussed initially. This work emphasized the design of CMOS op-amp model for low power, high gain, high-frequency applications. This work discussed various trade-offs between gain, bandwidth, phase margin, signal swing, noise, matching, slew rate and power consumption. The design of a single-stage OTA design is given in the paper. The stability with wide temperature was discussed in this paper.

After one year Wen-Whe Sue and et.al discussed the significance of folded cascode OTA in high-speed applications. Here the output capacitance is used for frequency compensation and width to height ratio is adjusted to improve output swing. This work exhibited 73dB(4.7K) open-loop dc gain and 1MHz unity-gain bandwidth[19].

In 1998 Henrik S and Sven M discussed an output stage with high linearity with the help of double-nested miller configured to provide low distortion[20]. The amplifier is designed in 800nm technology. The amplifier discussed in this work comprised of two stages namely input and output stage. The input stage is a differential stage with differential output and it is a transconductance stage. It is followed by the trans resistance output stage. This work consumed 130mW power from 3.6V supply.

In same year Jean-Paul E & team discussed the classical operational transconductance amplifier structures for applications up to 1GHz using 1µm technology[21]. The relations for open-loop gain, gain-bandwidth product and different poles are included to synthesize the circuit to obtain transit frequency for given load capacitance. The proper modelling of transconductance and substrate capacitance is included to design this high-frequency amplifier. Here the frequency was varied based on substrate doping level.

In 1999, Adrian R et.al designed an OTA using standard .35µm technology[22]. The designed circuit consumed 3mW from 2.5V power supply and obtained maximum linear input range of 250mV at a unity gain frequency of 100MHz.The improvement of large signal handling capacity of source coupled differential pair is done by increasing bias current and channel length or by decreasing channel width. Here the zero by mismatched differential pair is helpful to cancel the parasitic pole created by the folded cascode output stage.

In 2000 P.K. Chan and et.al discussed a novel systematic offset minimization circuit for designing a class AB CMOS operational amplifier[23]. Here the proposed circuit comprised of 4 parts. The four parts are the differential input stage, replica gain stage, Class AB output stage and biasing stage. The replica gain stage consists of biasing generator and a fully differential amplifier. Here the circuit is implemented .8µm CMOS technology. The total silicon area for the proposed amplifier was 3700 µm2.

In the same year, A.Younus&M.Hassoun discussed fully differential amplifier to improve open-loop gain[24]. Here the circuit used common-mode feedback circuit having switched capacitor. The circuit is designed in .25µm technology with 2.5 V power supply and obtained the response of 81dB gain, 680MHz unity gain frequency with the power consumption of 30mW power consumption.

Jyh-Neng Yang et.al designed a 2.4 GHz CMOS LNA in .35µm technology[25] in the year 2000.

The proposed circuit exhibited 33dB gain and consumed 17mW from 1.5V supply. The different performance parameters such as forward gain, noise figure, and s parameter obtained through simulation were discussed in the paper.

In the same year, Fernando S and Denis F presented a new class AB output stage without extra compensation capacitance [26]. Here two almost equivalent topologies were discussed in this work. The purpose of this work was to design an amplifier for battery-powered implantable medical devices. So utmost care was given to reduce power consumption

Again in the year, 2000 Po-Chiun Huang et. al. discussed a low voltage low power CMOS IF limiting amplifier [27]. Each gain cell of the proposed amplifier employed folded cascode amplifier to provide low voltage operation. The circuit exhibited 75dB gain, 10.7MHz UGB and consumed 6.2mW from 2V power supply. The amplifier is designed in .6µm CMOS technology and occupied active area of .4mm2.

J.Gilinianowicz et.al described a novel fully differential operational transconductance amplifier with high gain and bandwidth in the same year[28]. This work combined a linear cross-coupled quad input stage with an improved folded cascode circuit. The presence of a folded cascode amplifier increased the output resistance and gain without significant deficiency in bandwidth. This OTA was designed in SPICE level 3transistor model for 1.2µm AMI ABN CMOS process. Along with the design of the amplifier, the third-order elliptic filter was designed using the proposed amplifier as an example.

In 2001 ChangsikYoo and Qiuting Huang described a power amplifier for wireless application in .25µm CMOS technology[29]. This circuit employed class E topology and this topology helped to improve efficiency. A finite dc feed inductor replaced RF choke for high output power and efficiency. The soft switching property of class E amplifier minimizes power loss. Another design technique included in this work is a common gate switching scheme. This circuit delivered .9W output power to 50Ω load at 900MHz from 1.8V supply.

In 2002 Stanislaw S & Slawomir K suggested a simple technique to realize linear tunable operational transconductance amplifier[30]. The proposed circuit is simulated using MOS .5µm HP AMOS14TB process with LEVEL 7 parameters. Here a four-quadrant analogue multiplier is designed using the designed OTA. Monte Carlo simulations carried out in this work resulted in total harmonic distortion(THD) mean value as .31% and standard deviation of THD as .04%. The multiplier circuit consumed 5.8mW from 3.3V supply.

In 2003 Tang Tat H et al. designed a CMOS class E power amplifier for radiofrequency application fabricated using 250nm technology. Here the operating frequency is centred at 1.2GHz and 2.65GHz with 26dBm output power. Two amplifiers have been designed in this work, The first one is assembled as a chip on board using chip-to-PCB bond wires to implement high Q high current inductor. The second is housed in a standard package and it used on-chip bond wires to implement small and accurate inductor. The circuit achieved the power amplifier efficiency of 38% and operated at 2.65 GHz frequency[31].

In 2004 D.STANDAROVSKI et.al analysed the sample and hold circuit frequency response and dominant and non-dominant pole of each sub-circuits[32]. Stability of the circuit is studied on different temperature and process variations. Low voltage Rail to Rail operational amplifier is designed using AMS .6µm technology with 3.3V supply. For stabilization, miller capacitance is added in this work.

In 2005 Vincent K et al. suggested a power amplifier for 2.4GHz applications in 130nm technology[33]. In this work, sizing transistors was done without degradation of overall performance. The front end comprises of two stages with different transistors in cascode topology. The power stage consumed 550 mW from 2.5V. Considering overall performance the designed amplifier matched Bluetooth specifications.

In 2006 J. Chen et al. presented a frequency-dependent harmonic distortion analytical methods applicable to linear enhance OTA[34]. The analytical method proposed here predicted the design constraints for source degenerated highly linear OTAs. This method increased harmonic distortion components above MHz range due to parasitics. Three linearization techniques are proposed in this paper. Attenuation through floating gate MOS transistor is the first technique. The second linearizing technique is the source degeneration technique. Polynomial cancellation technique is used as the third linearizing technique. The floating gate MOS OTA improved linearity up to 10dB at 20MHz than equivalent OTA without FGMOS. This work concluded that the FGMOS OTA achieved high linearity at high frequencies with less power consumption

In 2007. Salvatore O C et al. proposed three different three-stage OTAs[35]. The first type of amplifier operated in Class A and it is used to describe the main approach. The main drawback of the first type is limited output drive capability and low voltage swing. The second architecture is tried to avoid the limitation of the first one by circuit modification and this modification increased the power consumption and output stage transconductance. To overcome this the designers moved to the third topology in which Class AB played a vital role.

In 2008 Kavita Khare presented a novel input and output biasing circuit to extend the input common-mode (CM) voltage range and the output swing. The mixed-signal circuits need to operate at low voltage levels[36]. In this work a newly designed input signal compression circuit was added to the input of a folded-cascode Op-Amp. The compression circuit equipped rail-to-rail input, while the folded cascode Op-Amp has rail-to-rail output. DC Simulation of folded cascode Op-Amp following the input signal compression circuit using cadence spectre showed that the rail-to-rail input the signal range is compressed to the common-mode range.

In 2011 Er. Rajni designed and analysed Folded-cascode the amplifier in 1.25 µm CMOS technology[37]. At first, the work described two-stage cascode op-amp design in 1.25 µm technology and it was found that the gain was not sufficient. As a remedy, the authors designed a high gain folded-cascode The simulation of the circuits was done using TSPICE simulation tool and the LEVEL–2,

1.25 µm parameters. A complete analysis of the circuit have done and the simulated circuits compared together. A comparison between the cascode and Folded-Cascode op amps is described. We have also described the comparison of their simulated and calculated results individually.

The designed circuit exhibited improved DC gain, improved ICMR and better PSRR.

In 2014 Jack Ou et al. proposed a low-noise folded-cascode amplifier to explain the tradeoffs using the gm/ID design flow[38]. A 130-nm CMOS process with a 1.2-V power supply was used for this work. The specifications are a slew rate of 7.5 V/µs, a load capacitance of 100 pF, a unity bandwidth of 10 MHz, an input/output common-mode voltage of 0.6 V, current consumption of 75 µA. The circuit required common-mode feedback (CMFB) with a bias current of 37.5 µA. The maximum device noise corner frequency was 20 kHz[38].

In 2015 YunYin et al. proposed a stacked 2.4-GHz CMOS power amplifier (PA) with a mode switching scheme. With the help of dynamically harmonizing the bias and optimal load with a power-detecting controller, the proposed mode switching scheme effectively improved the power-added efficiency (PAE) of the amplifier[39]. This work used the transistor stacking and envelope tracked self-biasing techniques, to improve power amplifier efficiency effectively. In 2017 Ramakrishna Kundu presented a two-stage fully differential, RC Miller compensated CMOS operational amplifier[40]. It could be used efficiently in a closed-loop feedback system due to high gain, and it is useful in high-speed applications due to its improved bandwidth. The circuit is implemented in 0.18 µm technology using the tool Cadence virtuoso. The designed circuit exhibited 95 dB gain, 135 MHz UGB, phase margin of 53^{o}, with 1 pF differential capacitive load. The circuit consumed 2.29 mW from 3.3V supply.

In 2018 Andrea et al.studied the electromagnetic effects at the input stage of low power, CMOS chopped operational amplifiers[41]. In this, the authors contracted the model to describe that chopped to study nonlinear distortion effects. Moreover, the proposed models are validated by using EMI susceptibility measurements and it showed simultaneous presence of the three types of offset in the same chopped operational amplifier.

In 2019 Ting Ma & Feng Hu presented a wideband flat gain LNA designed in 130nm CMOS technology[42]. Here the input matching is provided by an active inductor. The bandwidth obtained in this work was from 0.7 to 4.6 GHz the gain variation across the operating frequency is 1.3 dB. The circuit consumed 6.16 mW power with 1.4 V supply voltage.

Table- I: Summary of parameters in research works

Metrices	[17]	[25]	[27]	[40]	[42]
Gain(dB)	64	33	75	95	10.1
UGB(Hz)	200K	2.4G	10.7M	135M	4.6 G
POWER(mW)	2.5	17	6.2	2.29	6.16
Technology	1.2µm	350nm	600nm	180nm	130 nm
Supply Voltage	3V	1.5V	2V	3.3V	1.4 V

Performance parameters earned in remarkable research works are summarized in Table.1.Here we can witness the tradeoffs between parameters. As the application varies, the importance of the focused parameter changes. In the table, the highest bandwidth obtained is from[42] but the gain is poor in that design and it is with 130nm technology. But in [40] the gain improved to 95 dB with reduced bandwidth of 10.7MHz.For different design and technology, the value of performance is different. So the selection of design, topology and technology should be with care to get optimum performance.

III. CONCLUSION

This paper reviewed various CMOS amplifier architectures for high-frequency applications. Since CMOS technology has low power consumption ,it can be used widely for an amplifier. Tradeoffs between performance parameters are the main bottleneck in the design of an amplifier.In analogue communication, the amplifier is a major courageous block. The amplifier is subjected to different limitation such as bandwidth, dynamic range, settling time and stability due to the cutback of the supply voltage.

REFERENCES

1. YANNIS P TSIVIDIS,PAUL R GRAY,"An Integrated NMOS Operational Amplifier with Internal Compensation",IEEE Journal of Solid Sate Devices,Vol.SC-11,No.6,Dec 1976
2. WOLFGANG STEINHAGEN,WALTER L ENGL,"Design of Intergrated Analog CMOS Circuits-A multichannel Telemetry Transmitter,"IEEE journal of Solid State Circuits,Vol.SC 13,No.6 Dec 1978.
3. JEAN –CLAUDE BERTAILS,"Low frequency noise considerations fore MOS amplifier design,"IEEE Journal of Solid state Circuits",Vol.SC 14,No4 August1979
4. Paul R Gray,Robert G Meyer,"MOS Operational Amplifier Design- A Tutorial Overview.IEEE Journal of Solid State Circuits,Vol.SC-17,No.6,Dec.1982
5. 5.DAVID B RIBNER,MILES A COPELAND,"Design Techniques for Cascoded CMOS Opamps with Improved PSRR and Common –Mode Input Range",IEEE Journal of Solid State Circuits ,Vol.SC-19,No.6,DeC.1984
6. D.Ray,J.Gorecki,"Novel single ended CMOS Transconductance amplifiers", Electronic Letters,18th July 1985,Vol.21,No.15
7. J.A.Fisher,"A High-performance CMOS Power Amplifier",IEEE Journal of Solid State Circuits,Vol.SC-20,No.6,Dec.1985
8. Marc.G.R.Degrauwe, O.Nys, E.Dijkstra, J.Rijmenants, S.Bitz, B.L.A.G Goffart, E.A.Vittoz, S.Cserveny, C.Meixenberger, G.V.D.Stappen, H.J.Oguey, "IDAC:An Interactive Design Tool for Analog CMOS Circuits", IEEE Journal of solid-state circuits ,Vol.SC-22,No.6,Dec 1987.
9. G.Enpinosa,F.Montechi,E.Sanchez-Sinencio,F.Maloberti,"Noise Performances of OTA-C Filters", ISCAS'88
10. F.O.Eynde,W.Sansen,"Design and Optimization of CMOS wideband amplifiers", IEEE 1989 Custom Integrated Circuits Conference.
11. R.A.Sartschev,"Wideband Analog CMOS Circuits at Intermediate frequencies", Proceedings., Second Annual IEEE ASIC Seminar and Exhibit, 25-28 Sept. 1989.
12. O.Donoghue,M.Mallinson, P. Holloway,"A novel Programmable Gain Amplifier", Third Annual IEEE Proceedings on ASIC Seminar and Exhibit, 17-21 Sept. 1990.
13. T.Inoue,F.Ueno,Y.Aramaki,O.Matsumoto,M.Suefuji,"A Design of CMOS OTA's using simple linearizing techniques and their application to high-frequency continuous time filters, IEEE International Symposium on Circuits and Systems, June 1991,

14. R.E.Vallee,E.I.EI-Masry,"Novel CMOS operational amplifier design technique for high frequency switched capacitor applications,IEEEproceedings-G,Vol-138,No.5,October 1991
15. P.J.Crawley,G.W.Roberts,"Designing Operational Transconductance Amplifiers for Low Voltage Operation", IEEE International Symposium on Circuits and Systems, 3-6 May 1993, Chicago, IL, USA.
16. Anchada, Charoenrook ,Mani Soma,"A Linear Wide-Dynamic-Range BiCMOS Operational Transconductance Amplifier for High Frequency Applications", Proceedings of APCCAS'94, 5-8 Dec. 1994, Taiwan
17. E.Abou-Allam,E.I.El-A=Masry, "Design of Wideband CMOS Current-Mode Operational Amplifiers", Proceedings of ISCAS'95, 3 May 1995, Seattle, USA.
18. Jean-Paul E, Denis D.C,Paul.G.A,Jean-Pierre C,"Design of SOI CMOS Operational Amplifiers for Applications up to 300oC",IEEE Journal of Solid State Circuits,Vol-31,No2,Feb,1996
19. Wen-WheSue,Zhi-Ming Lin,Chou-Hai Huang,"A High DC-Gain Folded Cascode CMOS Operational Amplifier", Proceedings IEEE Southeastcon '98 'Engineering for a New Era, Orlando, USA, 24-26 April 1998
20. Henrik S, Sven M,"A 100 MHz CMOS Wide-Band IF Amplifier",IEEE Journal of Solid State Circuits,Vol.33,No.4,April 1998
21. Jean-Paul E, Denis F, Jean-Pierre R ,Jean-Pierre C,"Potential and Modeling of 1µm SOI CMOS Operational Transconductance Amplifiers for Applications up to 1GHz",IEEE Journal of Solid State Circuits,Vol-33,No.4,April 1998.
22. .Adrian R, Marius N, Oliver M,"CMOS Operational Transconductance Amplifier for PRML Read channel Applications", 1999 IEEE International Symposium on Circuits and Systems (ISCAS), Orlando, FL, USA, 30 May-2 June 1999
23. P.K.Chan,L.Sick,H.C.Tay,J.H.Su,"A Low Offset Class AB CMOS Operational Amplifier", IEEE International Symposium on Circuits and Systems SCAS 2000,May 28-31,2000,Geneva,Switzerland
24. A.Younus, M.Hassoun, "A High Speed Fully Differential CMOS Opamp",43rd IEEE Midwest Symposium on Circuits and Systems, Lansing MI,Aug.8-11,2000
25. Jyh-NengYang,Chen-Yi Lee,Terng-Yin Hsu,Terng-Ren Hsu,Chung-Cheng Wang, "A 1.5-V,2.4GHz CMOS Low-Noise Amplifier", 43rd IEEE Midwest Symposium on Circuits and Systems, Lansing MI,Aug.8-11,2000.
26. Fernando S,DenisF,"Analysis and Design of a Family of Low-Power Class AB Operational Amplifiers" , Proceedings 13th Symposium on Integrated Circuits and Systems Design (Cat. No.PR00843), Manaus, Brazil, Brazil, 18-24 Sept. 2000
27. Po-ChiunHuang,Yi-Huei Chen and Chorng-KuangWang,"A 2 –V 10.7 –MHz CMOS Limiting Amplifier/RSSI",IEEE Journal of Solid State Circuits .Vol.35,No.10,Oct.2000.
28. J.Gilinianowicz.J.Jakusz,S.Szczepanski,Y.Sun, "High-Frequency two-input CMOS OTA for continuous-time filter applications", IEE. Proc. Circuits Devices Systems, Vol.147,No.1,Feb,2000
29. ChangsikYoo,QiutingHuang,"A Common-Gate Switched .9-W Class-E Power Amplifier with 41% PAE in 0.25-µm CMOS".IEEE Journal of Solid State Circuits,Vol.36,No.5,May.2001
30. Stanislaw S,Slawomir K,"A 3.3V Linear Fully Balanced CMOS Operational Transconductance Amplifier for High-Frequency Applications", ICCSC'02. 1st IEEE International Conference on Circuits and Systems for Communications. Proceedings (IEEE Cat. No.02EX605), St. Petersburg, Russia, 26-28 June 2002.
31. Tang Tat H , Mourad N, El-gamal, "Class–E CMOS Power Amplifeirs for RF Applications", Proceedings of the International Symposium on Circuits and Systems, ISCAS '03. Bangkok, Thailand, 25-28 May 2003.
32. D.STANDAROVSKI,M.COUSINEAU,M.LESCURE,"Wideband,Low-Voltage CMOS Sample- and-Hold Amplifier Design", Instrumentation and Measurement Technology Conference, IMTC 2004,Como,Italy,18-20 May 2004
33. Vincent K,BaudouinM,Didier B,"20dBm CMOS Class AB Power Amplifier Design for Low Cost 2GHz-2.45GHz Consumer Applications in a .13µm technology", STMicroelectronics – Central R&D ,Crolles, France,2005
34. J.Chen,E Sanchez-Sinencio,J Silva-Martinez, "Frequency-Dependent Harmonic-Distortion Analysis of a Linearized Cross-Coupled CMOS OTA and its Application to OTA-C Filters", IEEE Transactions on Circuits and Systems-1,Regular Papers,V0l,53,March 2006.
35. Salvatore O C,Alfio D G,Rosario M, Gaetano P, SelvatoreP,"Design Procedures for Three-Stage CMOS OTAs With Nested –Miller Compensation",IEEE Transactions on Circuits and Systems-I Regular Papers ,Vol.54,No5,May2007
36. Kavita Khare,NilayKhare,Pawan Kumar Sethiya,"Analysis of Low Voltage Rail to rail CMOS Operational Amplifier Deisgn",IEEE International Conference on Electronic Design,Dec2008
37. Er. Rajni, "Design of High Gain Folded-Cascode Operational Amplifier Using 1.25 um CMOS Technology", International Journal of Scientific & Engineering Research Volume 2, Issue 11, November-2011.
38. Jack Ou, and Pietro M. Ferreira,"A gm/ID-Based Noise Optimization for CMOS Folded-Cascode Operational Amplifier", IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS—II: EXPRESS BRIEFS, VOL. 61, NO. 10, OCTOBER 2014.
39. YunYin,XiaobaoYu,ZhihuaWang,BaoyongChi,"An Efficient-Enhanced Stacked 2.4-GHz CMOS Power Amplifier With Mode Switching Scheme for WLAN Applications", IEEE TRANSACTIONS ON MICROWAVE THEORY AND TECHNIQUES ,VOL 63,NO.2,February 2015.
40. Ramakrishna Kundu,AbhishekPandey,SubhraChakraborty,VijaySingh,"A Current Mirror Based Two Stage CMOS Cascode Op-Amp For High Frequency Applications",Journal Of Engineering Science and Technology,Vol 12,No 3 .2017.
41. Andrea Lavarda,LucaPertruzzi,NejcRadez,BerdDeutschmann ,"On the Robustness of CMOS-Chopped Operational Amplifiers to Conducted Electromagnetic Interferences",IEEE Transactions on Electro Magenetic Compatability,Vol.60,No.2,April 2018
42. Ting Ma, Feng Hu , "A Wideband Flat Gain Low Noise Amplifier Using Active Inductor for Input Matching", IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS—II: EXPRESS BRIEFS, VOL. 66, NO. 6, JUNE 2019
43. Mahmood A. Mohammed; Gordon W. Roberts'' The Impact of the Scaled-Down CMOS Technologies on the Step Response Degradation Caused by the Pole-Zero Doublets in the OTAs", IEEE 11th Latin American Symposium on Circuits & Systems (LASCAS), San Jose,Costa Rica, 25-28 Feb. 2020

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